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1. GENERAL CHARACTERISTICS1.1. General

The C.P.U. GE 130 is an alphanumeric, digital and parallel processor for general use. It uses:

- decimal not signed arithmetics
- decimal packed and signed arithmetics
- binary arithmetics
- change registers and operations related to them.

It works on characters with 8 bits plus 1 odd parity bit. The memory has a maximum capacity of 32 768 positions. It can work with three channels for data transfer toward the outside, eventually overlapping. It uses the interruption sequence.

It is provided with 4 interface connectors for the connection with peripheral controllers, two of which are integrated and two standard.

The operator communicates with the processor through an operator panel which is located on a separate cabinet. In the same cabinet there are also the maintenance panel and the board-tester.

A power supply, sited in a separate wing, gives the volt ages required to make the C.P.U. and the connected peripheral units work.

The structures were designed according to the SMN standard.

The logic circuits consist of monolithic integrated circuits of the TTL type and of discrete components. The integrated circuits perform the NAND function and the NAOR (inverted And-or) function.

For more details refer to the "SCM3 Circuital Standard" publication with code no. 4.571.1.001.0/A.

The GE 130 can be connected to all the peripheral subsystems of the 115/2.

In addition, it is compatible with the 115/2 C.P.U. from the functional and structural point of view.

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1.2. Performances

The main characteristics are:

- elementary cycle of 2 μ s;
- maximum memory capacity: 32 768 characters;
- packed and signed multiplication and division done in hardware;
- operations with binary arithmetics;
- operations with decimal, unpacked and without sign arithmetics;
- operations with packed and signed arithmetics;
- possibility to change the addresses given in the program instructions, through 8 change registers corresponding to 16 memory positions (addresses 240 through 255);
- operations on the change registers;
- three eventually overlapped working channels.
 Channel 1, besides being in condition to perform data transfers with peripheral units, is specialized for all internal calculation; therefore, an external operation using channel 1 stops the execution of internal calculations.
 Channels 2 and 3 can only perform data transfer operations with peripheral units.
 For more details, refer to the logic for external instructions performance (see para. 2.7.);
- possibility to use the interruption sequence.

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1.3. Options and alternatives

The GE 130 C.P.U. is provided with the following options and alternatives:

- memory capacity which can be supplied in the following versions:

8 192 positions	UCE 460 (115/3)
12 288 positions	UCE 461 (115/3-120)
16 384 positions	UCE 462 (115/3-120-130)
24 576 positions	UCE 463 (120 - 130)
32 768 positions	UCE 464 (120 - 130)

- connectors enabled to program loading.

They can be two of the following connectors: 2, 3, 4;

- operating speed of the internal operations.

The cycle period can be of 2, 4, 6 μ s.

UCE 468 (130), UCE 467 (120), UCE 466 (115/3);

- connectors enabled to interruption.

They can be:

- none; (115/3 - 120 - 130)

- connectors 3 or 4 separately; (120 - 130)

- connectors 3 and 4; (120 - 130)

- hours counter for actual Power-ON (VAR 360 B).

It is enabled by the STAND-BY key on the operator panel.

The key is present; always fitted;

- In the 115/3 the performances added with respect to the 115/2. are always inhibited.

These alternatives and options, except those planned for the memory capacity and for the 2nd E.T.C. do not require the connection or disconnection of the related circuits, but they require the simple insertion of jumper boards.

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1.4.

Physical configuration

The GE 130 C.P.U. consists of the following parts:

- The CPU wing includes
 - timing logic
 - registers logic
 - logic sequence matrix
 - logic of control and of data transfer with the peripherals
 - magnetic core memory
 - ventilation devices
 - Console cabinet including:
 - operator panel
 - maintenance panel
 - board tester
 - Elapsed Time Counter (ETC) optional
 - Power supply wing including:
 - SCR +20VDC Power Supply
 - Switching Power Supply giving the voltages -20VDC, +12VDC, +5VDC.
- In these P.D.S. the power supply is not described.
Refer to publication n° 4.409.1.001.0/A, GE 130
Power Supply - Description.

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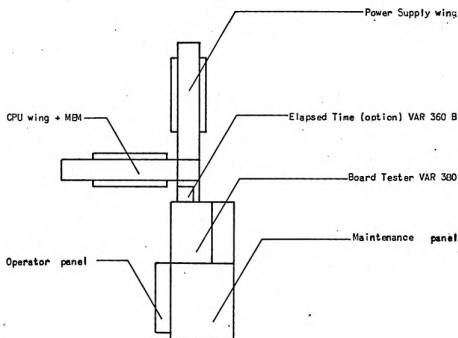
1.4.1. - GE 130 layout - Plan view

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1.4.2. Ventilation device (VAR 321)

The ventilation group is fitted in the base of the Central Processor.

It consists of three Boxer 208 + 230V 50+60 cycles fans assembled in a removable drawer.

It is provided with a thermoswitch protection system.

A heat dissipating resistance and thermoswitch assembly is mounted above each fan.

If the fan stops, the heat generated by the resistor is not dissipated by the rotating fan. This causes the thermoswitch to act, through which, within 7 minutes, the VAR 300 protection device is brought in to cut power. The VAR 300 is in the Power Supply wing.

The air flow yielded by every single fan must not be influenced by the other fans in order to allow the protections interventions.

For this reason, the air flow is split in two trunks.

1.5. Electrical and environmental requirements1.5.1. AC power supply

Two versions were planned:

1. 3-phase 220 Volts 50 cycles power supply
2. 3-phase 208 Volts 60 cycles power supply

In both cases, +10% variations on the voltage are allowed. The frequency can vary from +0.5 to -1.5 cycles for the 60 cycles power supply and +2 cycles for the 50 cycles power supply.

1.5.2. DC power supply

The power supply yields +20, -20, +12, +5 DC voltages and supplies the related overvoltage and overcurrent protections; for larger details refer to the Power Supply Description.

1.5.3. Temperature and humidity

- Under normal conditions, the subsystem can work with temperatures ranging from 10 °C to 38 °C (50 °F to 100 °F) with every relative humidity value ranging

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from 20% to 80%.

- In storing and shipping conditions, it can undergo temperatures ranging between -29 °C and +74 °C (-20 °F and 165 °F).

Note: the temperature and humidity variations must be such not to cause condensation.

- For the other environment requirements refer to:
"Common requirements to design GEISI products"
No. 300140030.

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2. GENERAL PROGRAMMING CHARACTERISTICS2.1. Instructions list

The GE 130 C.P.U. can perform the following instructions:

Note: an asterisk labels the instructions present in the previous versions of the Central Processor

LR : Load Register
 STR : Store Register
 AMR : Add Memory to Register
 SMR : Subtract Memory from Register
 CMR : Compare Memory to Register
 LA : Load Address
 * CMC : Compare Characters
 * NC : And on Characters
 * OC : Or on Characters
 * XC : Exclusive Or on Characters
 * MVC : Move Characters
 * CMI : Compare Immediate
 NI : And Immediate
 TM : Test under Mask
 OI : Or Immediate
 XI : Exclusive Or Immediate
 * MVI : Move Immediate
 * SR : Search Right
 * SL : Search Left
 * TR : Translate
 * AD : Add Decimal
 * SD : Subtract Decimal

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- * MVQ : Move Quartets
- * CMQ : Compare Quartets
- * AB : Add Binary
- * SB : Subtract Binary
- AP : Add Packed
- SP : Subtract Packed
- MVP : Move Packed
- CMP : Compare Packed
- MP : Multiply Packed
- DP : Divide Packed
- * PK : Pack
- PKS : Pack with Sign
- * UPK : Unpack
- UPKS : Unpack with Sign
- * EDT : Edit
- * JC : Jump On Condition
- * JRT : Jump Return
- * JS1 : Jump on Switch 1
- * JS2 : Jump on Switch 2
- * JIE : Jump on Internal Error
- * LON : Light On
- * LOFF : Light Off
- LOLL : Diagnostic Instruction
- * NOP2 : No Operation
- * INS : Inhibit Stop
- * ENS : Enable Stop
- LPSR : Load Program Status Register
- * HLT : Halt
- * PER : peripheral instruction
- * PERI : peripheral instruction with indirect unit name.

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2.2. Operation codes and instruction formats2.2.1. P format instructions

Symb.	Op.	2nd Chrt.	Quant. used implicitly	Description
ENS	*02	10 ✓	-	Enable Stop
INS	*02	20 ✓	-	Inhibit Stop
LOFF	*02	40 ✓	-	Light Off
LON	*02	80 ✓	-	Light On
NOP2	*07	X ✓	-	No Operation
HLT	*0A	X ✓	-	Halt
LOLL	02	81 ✓	-	Diagnostic Instruction

2.2.2. PM format instructions

Symb.	Op.	2nd Chrt.	Quant. used implicitly	Description
JRT	*41	MO ✓	Q, R7(1) (3)	Jump Return
JC	*43	MO ✓	Q (1)	Jump on Condition
JIE	*53	20 ✓	-	Jump on Internal Error
JS2	*53	40 ✓	-	Jump on Switch 2
JS1	*53	80 ✓	-	Jump on Switch 1
LA	68	RO ✓	-	Load Address
TM	91	K ✓	Q	Test under Mask
MVI	*92	K ✓	-	Move Immediate
NI	94	K ✓	-	And Immediate
CMI	*95	K ✓	Q	Compare Immediate
OI	96	K ✓	-	Or Immediate
XI	97	K ✓	Q	Exclusive Or Immediate
PERI	9C	X	Q, R7(2)	Peripheral Instruction (Indirect)
LPSR	9D	X ✓	Q	Load Program Status Register
PER	*9E	U	Q, R7(2)	Peripheral Instruction

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Symb.	Op.	2nd Chrt.	Quant. used implicitly	Description
STR	84	RO ✓	-	Store Register
LR	BC	RO ✓	-	Load Register
CMR	BD	RO ✓	Q	Compare Memory to Register
AMR	BE	RO ✓	Q	Add Memory to Register
SMR	BF	RO ✓	Q	Subtract Memory from Register

2.2.3. PMM format instructions

Symb.	Op.	2nd Chrt.	Quant. used implicitly	Description
MVC	* D2	L ✓	-	Move Characters
NC	* D4	L ✓	-	And on Characters
CMC	* D5	L ✓	Q	Compare Characters
OC	* D6	L ✓	-	Or on Characters
XC	* D7	L ✓	Q	Exclusive Or on Characters
UPK	* D8	L ✓	-	Unpack
SR	* D9	L ✓	Q, R7	Search Right
PK	* DA	L ✓	-	Pack
SL	* DB	L ✓	Q, R7	Search Left
TR	* DC	L ✓	-	Translate
EDT	* DE	L ✓	Q	Edit
MVP ✓	E8	L1 L2 ✓	Q	Move Packed
CMP ✓	E9	L1 L2 ✓	Q	Compare Packed
AP ✓	EA	L1 L2 ✓	Q	Add Packed
SP ✓	EB	L1 L2 ✓	Q	Subtract Packed
MP ✓	EC	L1 L2 ✓	Q	Multiply Packed
DP ✓	ED	L1 L2 ✓	Q	Divide Packed
PKS ✓	EE	L1 L2 ✓	Q	Pack with Sign
UPKS ✓	EF	L1 L2 ✓	Q	Unpack with Sign
MVQ ✓	* F8	L1 L2 ✓	Q	Move Quartets

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Symb.	Op.	2nd Chrt.	Quant. used implicitly	Description
CMQ	* P9	L1 L2	Q	Compare Quartets
AD	* FA	L1 L2	Q	Add Decimal
SD	* FB	L1 L2	Q	Subtract Decimal
AB	* FE	L1 L2	Q	Add Binary
SB	* FF	L1 L2	Q	Subtract Binary

Symbols used:

- * indicates the instructions of the basic set
- 0 - 9, A - F indicate hexadecimal quantities (in OP. and 2nd character)
- R indicates the name of a register
- M is the mask of the jumps on condition
- K indicates a character used as operand
- U indicates a name of Peripheral Unit
- X indicates an unused character
- L indicates a length expressed with 8 bits
- Q indicates that the instruction interests the qualitative
- R7 indicates that the instruction interests register No. 7.

NOTES:

- (1) It uses the qualitative, but it does not change it
- (2) Only the alternatives TPER (Channel 1) and SPER insert R7
- (3) In the basic set only M = F is allowed.

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NOTE: The positions left blank correspond to unused codes.

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2.3. Information structure2.3.1. Memory

Every position (or "character" or "word") in memory, which has its own individual memory address, is made up of 8 information bits.

The memory positions are numbered progressively starting from zero. The order number associated with a position is called "address", and is expressed in binary form.

A group of consecutive positions forms a memory "field". A field is defined by its length and by the address of its first position to the right or to the left.

(In the figures a field is always represented with a series of characters, the most significant ones to the left with the lowest addresses. In a position the most meaningful bits are represented to the left.)

All the memory positions are normally accessible by program; though, some are specialized for the following uses:

- a) change registers (they occupy addresses 240 - 255)
- b) store used by the multiplication and division instructions (address 232 - 239)
- c) store for the name of the peripheral unit, used by the instruction PERI (address 224)
- d) zone used by the interruption mechanism (addresses 768 - 775)
- e) two characters to the left of every zone used for the printing with an integrated line printer.

2.3.2. Data representation

The operands or "fields" written in memory have a variable length. The instructions refer to a field defining its address (equal to the last position to the left or to the right of the field itself) and its length, given in memory positions.

In the instructions the length of a field is normally defined as the distance between the two extremes of the field, and not as the number of positions occupied (the

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distance between the extremes of a field is equal to the number of position minus one).

The length can be given:

- by the content of the second instruction character; by varying from 0000 0000 to 1111 1111 it indicates the lengths from 1 to 256 characters;
- by the content of one of the two halves of the second instruction character; by varying from 0000 to 1111 it gives the lengths from 1 to 16 characters;
- implicitly: some instructions operate on fixed length fields (one or two or four characters depending on the instruction);
- by the content of the external sub-field.

Some instructions act on operands defined in an shortened form, as the change registers. The operands on which the instructions act can be considered as:

- a) - Alphanumeric operands, inclusive of the unpacked decimal operands
- b) - Binary operands
- c) - Decimal packed and signed operands

2.3.3.

Alphanumeric operands

An operand of this type consists of a sequence of "characters", occupying each one a position of the field.

Example:

A	B	C	1	2
---	---	---	---	---

A character is represented in the 8 bits of a position according to a "code".

The length of the operands of this type is variable, but cannot be more than 256 characters for internal type instructions.

The code to represent the data is normally, but not necessarily, the GECD given before.

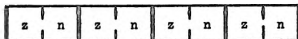
The decimal numbers form a special category of characters.

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In the codes normally used, the decimal numbers are coded with a fixed configuration in the 4 most significant bits (called "zone") and with binary values configurations in the 4 less significant bits ("numerical part") corresponding to the numbers.

A sequence of characters of this type, with a length between 1 and 16 words, represents a decimal number in "unpacked" form, suitable to be processed arithmetically by the instructions AD, SD, MVQ, CMQ.

The format is of the type:



in which:

n = Decimal number in pure binary code, from 0000 to 1001.

The other combinations, if processed arithmetically, give a definite result and allow the instructions to be executed normally.

z = Zone. Every combination is accepted as zone. Normally the combination 0100 is used.

The combination 1010 on the less significant character can be used to indicate a negative sign.

Instructions AD, SD, MVQ, CMQ consider the decimal unpacked numbers as whole positive numbers, and do not use or change the zones.

The PKS instruction interprets as a negative sign the combination 1010 in the zone of the last character to the right, and as a positive sign any other combination.

The UPKS instruction always generates, on all the digits, the zone 0100.

2.3.4.

Binary operands

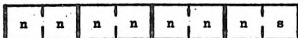
The content of the fields reserved to operands of this type is considered generally as a sequence of bits, used as such. The length of the binary operands can be variable, but cannot be above the 256 positions.

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2.3.5.

Decimal operands

The operands of this type are represented in "packed" and "signed" form, i.e. every memory position contains two decimal characters, and every operand contains a sign code in the right half less significant position.



n = Decimal number, in pure binary code, from 0000 to 1001
The other combinations, if processed arithmetically, give a definite result and always allow the instructions to terminate normally.

s = Sign. The values 1011 (hexadecimal B) and 1101 (hexadecimal D) are interpreted as negative sign. All the other combinations are interpreted as positive sign. When the operations generate a new sign, they always create the configuration 1100 (hexadecimal C) as positive sign, and 1101 (hexadecimal D) as negative sign.

The decimal operands may have a variable length, but they must not be above the 16 memory positions.

If L is the decimal field length, L + 1 is the number of memory positions occupied by the decimal operand, and the number of digits of the operand is (2L + 1), always odd. These operands can be processed arithmetically with the instructions AP, SP, MVP, CMP, MP, DP.

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Cod. 3300123

P

OP	C
----	---

PM

OP	C	I1
----	---	----

PMM

OP	C	I1	I2
----	---	----	----

The different length depends on the number of memory fields to which the instruction itself refers.

A particular code is present for each instruction which gives the type of operation (OP) and an auxiliary character, termed (C).

In addition, there can be no field address, only one address or two depending on the format.

The OP code (type of operation) occupies one memory position, and specifies the following information:

- a) - Type of operation to be performed
- b) - Format of the instruction

The auxiliary character C occupies one position. The meaning and the function of the auxiliary character differs according to the type of instruction: it can indicate the length of the operands, or the registers to be used, or to further specify the type of operation. The addresses used in the instructions define the memory positions of the operands on which the instruction itself will be performed.

In the two address format, the operands will be defined with the name of "first operand" and "second operand", defined by the first and second address respectively. Every address occupies two memory positions. Two different address structures are possible, "absolute" and "modified". Bit 15 of each address indicates the structure of the address itself. If the bit value is one, the address is modified, if it is zero, the address is absolute.

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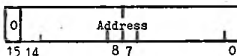
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If the letter M represents a modified address and A represents an absolute address, we may say that:

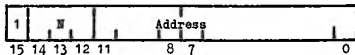
- There are two possible structures, A and M for single address instructions
- There are 4 possible structures, AA, AM, MA and MM for two address instructions.

2.5.1. "Absolute" address



The content of the two positions specifying the address of the operand is used directly as the address of a position, or of a memory field. The 15 available bits can address up to 32 768 memory positions, with addresses from 0 to 32 767.

2.5.2. "Modified" address



In this case, the content of the bits 14 through 12 of the first position of the address is interpreted as the name of one of the 8 change registers. The address of the operand is obtained adding to the content of the given register (considered as "basis" of the addressing) the value of the remaining 12 bits of the address. The sum is done on the length of the register (2 words), with the loss of the carry over beyond the 2nd word.

2.5.3. Invalid addresses

Independently from the size, the memory operates on words written with consecutive addresses going from zero to M - 1, if the words written are M.

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Any access to words with a higher address, for internal or external operations, determines, when writing, the loss of information and, when reading, the reading of the fixed configuration 0000 0000. In both cases, anyhow, the signal of "Invalid address" is given and the machine stops.

Note: All the programs, written for the previous versions of the Central Processor, which are not using invalid addresses and do not take advantage of the storage address circularity, can work on the GE 130.

2.6. The qualitative results

Some instructions, beside operating on the data held either in memory or in the machine registers, also operate on two flip-flop (RIPO and DIVE) which give a "Qualitative result".

The Qualitative Result consists of the presence of one of four alternatives, mutually exclusive, loaded at the end of the instructions (e.g. result of an arithmetic operation positive or negative or null or incorrect because of insufficient capacity of the result storing field. The meaning of the four possible results will be explained at every instruction.

The Qualitative Result is normally used, examining it with Jump instructions, to create deviation from the normal program sequence.

From the qualitative result point of view, FA04 and FA05 correspond respectively to RIPO and DIVE in the 115/1 and 115/2.

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2.7.

The external operations

All external instructions used by previous GE 115 models are included and compatible with the present program organization of the GE 130.

The compatibility is guaranteed for the programs written in compliance with the rules mentioned in the manuals for the central processor.

The GE 130 has, when compared with previous Central Processors, a far greater possibility to operate on external instructions in overlap mode.

2.7.1.

Connectors

For the connection to the peripheral units (P.U.), the GE 130 has 4 connectors: two integrated (1 and 2) and two standard (3 and 4); the following controllers may be connected to these connectors:

- Connector 1
 - parallel printer (up to 600 lines per minute) integrated version or
 - MB serial printer standard version.
- Connector 2
 - serial card reader (up to 600 cards per minute) integrated version
 - magnetic characters document reader integrated version
- Connector 3
 - any single or multiple controller with standard GE 100 interface, or according to specifications 300740110, or
 - a Multi Peripheral Adaptor, through which it is possible to connect 4 different controllers, with a maximum of 64 peripheral units.

This connector may be enabled to receive the interrupt signal, when the system is installed.
- Connector 4

It has the same performances of connector 3. In addition, in connection of the line controllers of the type Datanet 9, 10/11, 12 this connector allows the use of

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the device "permission to disconnect" (P.P.S. 300740210).

2.7.2. Channels

The C.P.U. communicates with the controllers connected to the connectors, through three channels called 1, 2 and 3 which are different for:

- connectable connectors;
- allowed overlapping;
- maximum frequencies of characters exchange.

The possible connections of a connector to a channel, which can be done through instructions are:

CHANNELS

	1	2	3
1	* (1)	* (2)	* (1)
2	*	*	*
3	*	-	*
4	*	-	*

CONNECTORS

- (1) only the controller of the serial printer
(2) only the controller of the integrated printer

Every channel can work connected to one connector at a time.

2.7.3. Names of the peripheral units

Every peripheral unit has a name which is a 8 bit code. The names of the units depend on the connectors by means of which their controllers are connected at the moment of the installation, according to the following correspondence:

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Connector	Unit name
1	11000000
2	10000000
3	00XXXXXX
4	01XXXXXX

The less significant bits may assume the following values, in the case of connectors 3 and 4:

- for controllers directly connected to the connector they represent the code of one of the 64 units of the controller;
- for controllers connected through a Multi Peripheral Adaptor they represent in part (2 bits) the code of the controller within the Multi Peripheral Adaptor and in part (4 bits) the code of one of the 16 units within the controller:

connector of the Multi Peripheral Adaptor	Name of the unit (6 less significant bit)
1	00XXXX
2	01XXXX
3	10XXXX
4	11XXXX

Within a multiple controller the units are numbered in progression, and in certain cases, the name can be assigned by the operator.

2.7.4. Priority

A priority order has been fixed between the requests of characters exchange of the channels.
It is:

Channel	Priority
1	Top
3	Medium
2	minimum

The priority of a channel has a considerable importance on the maximum characters exchange frequencies, when the work is done with overlapping of several channels.
The priority of a controller, and therefore of a connector

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depends on the priority of the channel to which it is associated.

2.7.5. Allowed overlappings

The operations described at points a, b and c below may be performed in overlap mode. Transfer frequency limitations are not considered.

- a) transfer of characters on channel 1 or internal calculation;
- b) transfer of characters on channel 2;
- c) transfer of characters on channel 3.

When operating on channel 1, internal calculations can not be overlapped to character transfers.

It is possible to start channel 2 in a not overlapped way with calculation, and channel 1 in such a way that the calculation is blocked up to the end of operations on channel 1 and 2. In this way, using the software of the 115-1 or 115-2, the overlappings are reduced exactly to the ones of the 115-1 and 115-2.

2.8. Instructions performance

A general internal instruction is performed in two distinct phases.

In the first phase, called phase α , the characters forming the instruction itself are read and interpreted.

In the second phase, called phase β , the instruction is actually carried out.

The external instructions are instead performed in three phases:

- 1) Phase α similar to that for internal instructions
- 2) Phase β general which interprets and stores the subfield of the instruction
- 3) Phase β of effective performance.

Some types of external instructions do not have the phase β of effective performance.

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2.9. Listing of all the operating times

All the given times refer to a memory cycle of nominal 2, 4, 6 μ s (respectively for 130 - 120 - 115/3).

Instruction	115/3 (μ s)	120 (μ s)	130 (μ s)
Address indexing	-	8	4
LR, STR	-	28	18
AMR, SMR, CMR	-	36	22
LA	-	20	14
XC, NC, OC	18+18N	16+12N	14+6N
CMC	18+18C	16+12C	14+6C
MVC	18+12N	16+8N	14+4N
CMI	32	24	16
OI, NI, XI, TM	-	24	16
MVI	26	20	14
SR, SL	30+18C	24+12C	18+6C
TR	18+18N	16+12N	14+6N
AD, SD, CMQ, MVQ,			
AB, SB	18+18N	16+12N ₁	14+6N ₁
AP, SP (without complement)	-	20+12N ₁	16+6N ₁
Complementation	-	10+12N ₁	4+6N ₁
MVP	-	20+8N ₁	16+4N ₁
CMP	-	20+12N ₁	16+6N ₁
DP*	-	10-80N ₂ +	11-40N ₂ +
		154(N ₁ -N ₂)+	77(N ₁ -N ₂)+
		182N ₂ (N ₁ -N ₂)	91N ₂ (N ₁ -N ₂)
MP*	-	18-48N ₂ +	15-24N ₂ +
		76(N ₁ -N ₂)+	38(N ₁ -N ₂)+
		126N ₂ (N ₁ -N ₂)	63N ₂ (N ₁ -N ₂)
PK	18+24N ₁	16+16N ₁	14+8N ₁
PKS	-	16+16N ₁	14+8N ₁
UPK	18+18N ₁	16+12N ₁	14+6N ₁
UPKS	-	16+8N ₁	14+4N ₁
EDT	18+18N ₁	16+12N ₁	14+6N ₁
JC	14	12	10
JRT	26	20	14
JS1, JS2, JIE	14	12	10
LON, LOFF, NOP2,			
IHS, ENS	10	8	6
LPSR	-	24	16
Interruption	-	40	20

UNIT

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* APPLIC.

CONT. SU FD. 28 NO. 27

N : number of words in the operands field
 NI : number of words in the first operand field
 N2 : number of words in the second operand field
 C : number of words actually explored.

* NOTE: These are average values, calculated assuming that multiplicand, multiplier and quotient have digits with an average value equal to 4.5.

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3. OPERATOR PANEL

The operator panel includes the push-buttons and the lights required by the operator to use the machine. Here below definitions are given for the functions of the keys, the meaning of the lights, and some operator manœuvres.

The operator panel is mounted in cabinet separate from the Central Processor to which it is connected through cables.

The following description considers the console as divided in different zones from the functional point of view.

3.1. Switching ON and OFF

Key to switch the system OFF: it disconnects the whole system from the power supply. It has no associated lights, it is opaque, red and has nothing written on it.

~ ON: this key connects the system to the A.C. mains. It has no associated lights.

D.C. ALERT - POWER OFF: this key switches off the Central Processor power supply and the power supply that produces the system centralized D.C. voltages.

Two lights are associated to the key:

- a yellow (POWER OFF) light, indicating the presence of the A.C. voltage at the power supplies input in OFF conditions;
- a red (D.C. ALERT) light, which is switched on with the POWER OFF light when the system is switched off for a malfunction (overtemperature, etc.).

POWER ON: with the system connected to the mains and no failures present (POWER OFF lit and DC ALERT out), the pushbutton POWER ON switches on both the CPU Power Supply and the centralized DC Power Supply.

A yellow indicator show, when lit, the machine ON condition.

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STAND BY: it is a switch with a blue light associated. It is always present but it is only enabled when the optional ETC is fitted.

- When the switch is not inserted the associated light is off. In this condition, the Start Key starts the machine operation, and the Counter advances until the machine is switched off or STAND BY is pressed. The ability to stop the counter, when the Central Processor stops (HALT light on), starting it again at every START has been built in the machine, but it is not presently enabled.
- When the STAND BY switch is inserted, the associated light is on. In this condition, the START key does not start the machine, and the Counter does not work. It is possible to unlock the Central Processor with a special key, in order to use it without advancing the Counter for performing maintenance operations.

3.2.

Signals

MEM CHECK - INV ADD: it is a double red light: the upper part (MEM CHECK) signals the detection of a disparity error on data read from storage; the lower part (INV ADD) signals that a memory cycle has been requested for a non-existing address.

MAINT ON - LAMPS CHECK: MAINT ON is a red light, which is switched on when one of the switches of the maintenance panel is in a position that does not allow the normal machine operation. The LAMPS CHECK key is associated to this light; this key lights all the lights of the console not enabled by keys, for testing purposes. This test must not be done during machine operation.

3.3.

Operation

STEP-BY-STEP: this STEP-BY-STEP key enables the machine to execute the instructions step-by-step one for each pressure of the START key. The associated white light indicates that the switch is inserted.

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During the step-by-step operation, the address and the function code of the instruction that will be performed next are displayed on the console.

The switch may be tripped in the middle of a program run to induce the program to stop at the end of the instruction under way.

The INS instruction inhibits the function of this switch. The function is enabled again by the ENS instruction or by the CLEAR key or by the STOC switch on the maintenance panel.

CLEAR key: it stops the execution of all the operations under way in the subsystem, and resets all existing error conditions.

It presets the Central Processor and the Peripheral Units in a well defined condition, irrespective of the previous statuses.

This is necessary especially after an error of the type MEM CHECK or after the system has been switched on.

The first pressure of START after CLEAR causes the following operations:

- a) if other switches are not inserted the execution of the program starts again; the address and the initial conditions are forced at a fixed value (refer to para. 5.3.2.);
- b) if the LOAD switch is inserted, the program loading is executed (refer to para. 5.3.).

The operation a) is meaningless if the storage content is unknown, such as after the machine has been switched on or after the machine was stopped with CLEAR during the program execution.

No light indication is associated to the key.

LOAD1/LOAD2: the LOAD1/LOAD2 switch has associated a double white light indicating its position. It allows to select one between two peripheral units enabled, during installation, for program loading.

LOAD: the LOAD key prepares the execution of the program loading, i.e. the loading of an initial program block from peripheral unit and the starting of its execution.

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			LOC. Pregnana	
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The sequence of loading operations is:

- CLEAR
- Preparation and selection of the required peripheral unit
- LOAD
- START

In the chapter dealing with program loading (5.3.) the functions of the above mentioned operations are described in detail. No light is associated to the LOAD key.

HALT - START: the START key starts the operations. The associated light (HALT), white, indicates that the machine has stopped, because of an HLT instruction; or because of the STEP-BY-STEP key, or through operations on Maintenance Panel...

SWITCH1 and SWITCH2: These are two switches, whose positions can be tested by program (JS1, JS2 instructions). The associated lights indicate the switch positions and are on when the conditions are at the logical value "1" (that causes the execution of jumps JS1 and JS2 respectively).

OPER. CALL: it is a blue light, switched on by the program with the LON and LOLL instructions to call the operator. The light is switched off by the LOFF instruction or by the CLEAR key.

3.4. Performance conditions

Two rows of 16 bit lamps display the content of the B0, F0 registers and some machine conditions.

With the machine in Halt condition and the Maintenance Panel switches in normal position, they show:

Upper Row: the bit lamps give the address of the 1st character of the instruction that will be executed next (ADD.REG., B0 register).

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Lower Row from left to right:

- 4 bit lamps indicate the program conditions:
 - first jump condition (OF, FA04 signal)
 - second jump condition (NZ, FA05 signal)
 - interrupt mask (IM, FA06 signal)
 - jump instruction executed (JE, AVER signal)
- 4 bit lamps indicate conditions concerning the external operations:
 - interruption present (I, INTE signal) RINT
 - channel 1 busy or CFU waiting (C1, PUC1)
 - channel 2 busy (C2, PUC2)
 - channel 3 busy (C3, PUC3)
- 8 bit lamps show the operation code of the instruction that will be executed next (OP.REG., FO register).

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4. MAINTENANCE PANEL

The Maintenance Panel is located in the same cabinet of the Operator Panel and access is gained to it by lifting off the pressure mounted covering panel. Through the switch and rotary selector mounted on the panel, data may be introduced in memory or particular machine registers. Configurations in registers and memory may be visualized and the execution of some operations can be modified or conditioned.

4.1. Signals

R000 to R008 display the R0 register
 S000 to S007 display the S0 register
 FA00 to FA03 display the first 4 bits of the FA register
 UR displays the URPE FF
 B1 to B4 display the selection of the 4 connectors
 SA00 to SA07 display the SA register

4.2. Operation keys and switches

PAPA - Switch - It causes the step-by-step execution of the microsequences of the Central Processor (after each step is performed), without interfering with the transfers from peripheral unit.
 START starts the execution of a step.

PATE - Switch - It stops the timing after every cycle of the delay line. START starts the timing for a cycle.

RICI - Switch - It disables the execution of the commands loading next Status, allowing to repeat the execution of a Status.

ACOV - Switch - It stops the machine when a jump condition is verified at the end of the reading of the Jump instruction.

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ACON - Switch - It stops the machine if the jump condition is not verified, at the end of the reading of the Jump instruction.

STOC - Switch - It enables to stop the Central Processor, with the Step-By-Step Switch, even if the Step-By-Step mode has been inhibited by the program.

INAR - Switch - It inhibits the stopping, should there be a check error in reading from memory or should the memory be addressed at a non-existing address.

INCE - Switch - It inhibits the correction of the check bit for the characters arriving from external units. When a forcing in storage is performed from console. This switch causes AM08 to be stored as an odd parity bit, inhibiting the generation of the check for the character stored from switches AM07 to 00.

SITE - Switch - When it is inserted, the Central Processor will not wait for the availability or the triggers from the external units, allowing the program to evolve normally.

LAMPS - Switch - It has three positions:

- 1 - OFF (normal position): all the lamps of the maintenance panel are off
 - 2 - ON: It powers the lamps above mentioned
 - 3 - DIAG: It powers the lamps above mentioned, sets the unit in diagnostic mode, and powers MAINT ON.
- Switches AM00 through 15 are used either to load or to visualize configurations on the main machine registers.
- Rotary switch.

Used to load and/or visualize configurations in main machine registers and memory.

With machine stopped, the various positions of the switch give visual access to the various registers through BO as shown in the following list.

This operation is possible by the fact that the Logic Sequence Matrix (LSM) is still receiving timings by the cycling delay line.

When START is pressed, the MLS performs instead a forcing cycle in the register under exam through switches AM00 to 15.

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4.3.1. Remote Control Rig

It is a rig employed to carry out functions on peripherals when it would be time consuming or impossible to utilize console commands.

It houses and duplicates the following keys: CLEAR, START and STEP-BY-STEP.

It is connected with ample cable length to the console and has a light incorporated to STEP-BY-STEP to denote its activation. Under these conditions, the lamp MAINT ON, located on the Operator panel also lights.

In these conditions, also the MAINT ON lamp of the operating console switches on.

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4.4. - Maintenance panel layout

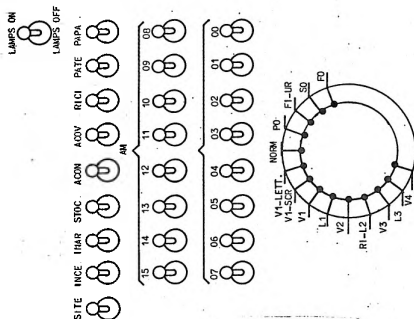


Fig. 3

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REVISION

5. FUNCTIONAL DESCRIPTION5.1. The program parameters

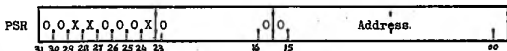
The program performance consists of the reading, recognition and subsequent execution of the instructions. The current instruction address and all the quantities which can condition its performance, form the "program status".

During the program execution the status evolves: the address of the program is increased following the instructions performed in progression and is varied by carrying out branch instructions.

Certain instructions and the interrupt process can change completely the program status.

The program status is kept in various machine registers, called generally PSR (program status register).

The PSR structure is the following:



This representation is symbolic.

Bit 29: consists of the FA04 flip-flop content

Bit 28: consists of the FA05 flip-flop content

Bit 24: consists of the FA06 flip-flop content. When it is at "1", interruptions are not considered.

5.1.1. Address

It is the address of the program being carried out. In other words, is the address of the OP word of the instruction which is to be performed and which is stored in PO register. This representation serves only to show how the PSR will be unloaded in the auxiliary memory zones OP SR and IP SR, detail which will be examined further on in the text.

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5.1.2. The program run

The program run is normally sequential in time, i.e. the interpretation of an instruction occurs as soon as the previous instruction is over or simultaneously to it in case of overlapping.

The following cases are an exception to this behaviour:

- a) during the instruction an interrupt is generated or acknowledged. In this case the interrupt is executed before interpreting the following instruction;

- b) The operator console "STEP-BY-STEP" switch is inserted.

The interpretation of every instruction is interrupted at the beginning, stopping the program performance; It starts again when START is pressed.

The instruction is performed or an interruption which may be enabled meanwhile, is served.

The switch "STEP-BY-STEP" is again checked at the beginning of the following instruction. There is also an HLT instruction, which causes an interruption in the program run and can be considered as an instruction with an execution phase with an undefined length, which is finished by pressing START.

The interruption due to the "STEP-BY-STEP" switch or to the HLT instruction, occurs after reading the function code of the instruction, with the program addresser still on the OP code of the instruction just read. The effect of the "STEP-BY-STEP" can be inhibited or enabled by program, through instructions INS and ENS.

5.2. Interruption5.2.1. Organization of the specialized storage zone

The specialized storage zone includes two buffers used for the interruption performance.

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The buffers are:

Decimal Address	Hexadecimal Address	Name	Description
768+771	0300 + 0303	OPSR	"Original Program Status"
772+775	0304 + 0307	IPSR	"Interrupt Program Status" register

The use of these two areas is explained in the following paragraph.

5.2.2. Interrupt procedure

The interruption is a discontinuation in the program performance, introduced between the end of an instruction and the beginning of the following one, with the following procedure:

- storage in memory, in the OPSR zone, of the content of the PSR status register;
- PSR loading with the content of the IPSR zone;
- starting again of the program.

5.2.3. Interrupt causes

Only special standard peripheral subsystems can issue an interruption signal.

During installation, the subsystems enabled to cause an interruption can be chosen: all the others remain inactive from this point of view.

The interruptions are felt and performed only if the bit 24 of PSR (FA06) is at the "0" value. Otherwise, they stay inactive.

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Notes

The program must perform an LPSR instruction, loading the interruption mask (bit 24 of the PSR) with the value "0" in order to enable the interruptions.

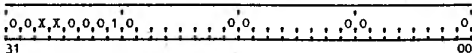
Once the interruption has been served (this will normally imply the performance of external instructions, eliminating the interruption condition), a LPSR instruction with address 768 (OPSR) will allow to re-start the performance of the interrupted program and to enable again the interruption conditions.

Program Loading

Initial loading of the program

This operation causes, when START is pressed, the following operations:

- Forcing in PSR of the quantity:



The created address is 0000.

- Selection of a peripheral unit of the system.

During installation, two peripheral units for program loading must be chosen among the three with the following names:

0000 0000	Standard connector (3)
0100 0000	Standard connector (4)
1000 0000	Integrated connector (2)

5.4. Internal instructions5.4.1. General

The GE 130 internal instructions can be divided in two well defined groups:

- 1 - basic instructions, equal to the ones of the previous version of the Central Processors;
- 2 - additional instructions: packed and signed arithmetics, with multiplication and division; operations on change registers; logic operations of immediate type.

5.5. Basic set of internal instructions5.5.1. Decimal arithmetics

All the decimal arithmetics instructions of the basic set operate on unpacked data and have a 2-address format:

OP	L1	L2	I1	I2
----	----	----	----	----

- OP : type of operation
 L1 : binary number indicating the length of the first operand, equal to L1+1 positions (from 1 to 16)
 L2 : binary number indicating the length of the second operand, equal to L2+1 positions (from 1 to 16)
 I1 : address of the rightmost byte of the first operand (indexable or not)
 I2 : address of the rightmost byte of the second operand (indexable or not)

Both operands are detected through the address of their less significant position, and all the operations are performed position by position, from right to left. The operands are assumed to be positive integers, right aligned.

Only the case $L2 \leq L1$ has a practical interest: for $L2 > L1$ everything occurs as if $L2 = L1$. If $L1$ is greater than $L2$, it is assumed to increase to the left the second operand with all zeroes.

The "zones" of the characters are not processed.

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5.5.1.1. Add Decimal - AD

The second operand is added to the first operand, and the sum is placed in the first operand location. A possible carry-over to the left of the first operand is lost (overflow).

The zones of the first operand and the second operand are not altered.

Qualitative Result:

FA04 FA05

0	0	Sum is zero
0	1	Sum is different, from zero
1	0	Overflow - partial result equal to zero
1	1	Overflow - partial result different from zero

5.5.1.2. Subtract Decimal - SD

The second operand is subtracted from the first operand and the difference is placed in the first operand location. The zones of the first operand and the second operand are not altered.

If the result is negative, it is stored in complemented form (complemented to $10^{(L1+1)}$).

Qualitative Result:

FA04 FA05

0	0	Not possible
0	1	Difference is less than zero (complemented)
1	0	Difference is equal to zero
1	1	Difference is greater than zero

5.5.1.3. Move Quartets - MVQ

The content of the field, given as second operand, is moved to the field of the first operand, maintaining, though, unchanged the zones. Also the second operand is left unchanged by the operation.

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The operands are assumed to be positive binary integers right aligned.

For practical purposes, only the case $L2 \leq L1$ is interesting: if $L2 > L1$ the instruction is executed as if $L2 = L1$. If $L2 < L1$, the operation is executed as if the second operand was prolonged to the left with all zero bits.

5.5.2.1. Add Binary - AB

The first operand is added to the second operand, and the sum is placed in the first operand location. The operation is performed with the loss of a possible carry-over beyond the length of the receiving field (overflow). The second operand is not altered.

Qualitative Result:

FA04 FA05

0	0	Sum is zero
0	1	Sum is different from zero
1	0	Overflow and partial result equal to zero
1	1	Overflow and partial result different from zero

5.5.2.2. Subtract Binary - SB

The second operand is subtracted from the first operand and the sum is placed in the first operand location. If the result is negative it is stored in complemented form (complemented to $2^8(L1+1)$). The second operand is not altered by the operation.

Qualitative Result:

FA04 FA05

0	0	Not possible
0	1	Difference less than zero (complemented)
1	0	Difference equal to zero
1	1	Difference greater than zero

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5.5.3. Alphanumeric instructions

All these instructions have a 2-address format:

OP	L	I1	I2
----	---	----	----

OP : type of operation

L : binary number indicating a length equal to L+1 characters (from 1 to 256)

I1 : address of the leftmost byte of the first operand (indexable or not)

I2 : address of the leftmost byte of the second operand (indexable or not)

This group includes the following instructions: Move, Compare, Translate, Format conversion, Edit and all logic operations.

These instructions can operate on binary or alphanumeric data.

The Auxiliary Character can contain, depending on the cases, the length of both the operands or only the length of the operand defining the termination of the operation. All these instructions are executed byte by byte, from left to right.

Both the operands are addressed by means of the address (I1 and I2) of their most significant position.

5.5.3.1. Move Characters - MVC

The second operand is placed in the first operand location.

The length of both the operands is L+1 bytes. The second operand is not altered.

The fields may overlap: movement is from left to right through each field a byte at a time.

Qualitative Result: it is not interested.

5.5.3.2. Compare Characters - CMC

The operands contained in the two fields, both of L+1 characters, are compared and are not altered by the operation. Comparison is purely binary.

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The indication of equality and difference has always a meaning between alphanumeric fields; the majority and minority relationship has a meaning only if the code which is used has an order of importance, i.e. it assigns binary configurations of higher order to the most significant characters in a comparison; the GECD code complies with this rule.

The operation proceeds from left to right and ends as soon as in both fields an inequality is found: they are explored totally only if the fields are equal or differ only in the rightmost byte.

Qualitative Result:

FA04 FA05

0	0	Not possible
0	1	First operand smaller than the second
1	0	First operand equal to the second
1	1	First operand greater than the second

5.5.3.3. Translate - TR

The instruction uses the second operand as "table" for the transcoding. Every byte of the first operand is substituted by the content of a location of the table adding the binary value of the byte of the first operand to the address of the second operand.

The operation proceeds from left to right, one byte at a time. The auxiliary character of the instruction indicates the length of the field to be transcoded, i.e. the first operand. The effective length of the second operand depends on the extension of the set of characters to be transcoded. The second operand is not altered. The address of the second operand must be an integer multiple of 256.

Qualitative Result: it is not interested.

5.5.3.4. Pack - PK

The format of the second operand, considered as unpacked, is changed to packed and transferred to the field of the first operand. The first address indicates a field L+1 positions long, destined to receive the result.

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The operation proceeds from left to right, and the result is obtained loading in a packed form the 2L+2 less significant halves of the characters of the second operand. The "zones", i.e. the most significant halves of the characters, are not considered. The signs are not processed.

The second operand is not altered.

Qualitative Result: it is not interested.

5.5.3.5. Unpack - UPK

The format of the second operand, considered as packed, is changed to unpacked and transferred to the field of the first operand. The second operand is a field L+1 positions long, which is not altered by the operation. The characters of the second operand are read from left to right; they are being expanded and each group of 4 bits goes to occupy the less significant half of one of the 2L + 2 positions of the receiving field, completed in the most significant half by the pre-existing "zone" code. The signs are not processed.

Qualitative Result: it is not interested.

5.5.3.6. Edit - EDT

The first operand initially contains the pattern controlling the execution of the instruction. Subsequent to the operation, the operand is cancelled and replaced by the result.

The second operand consists of one or more fields, normally unpacked decimal, to be edited and is not altered. The auxiliary character of the instruction specifies the length of the pattern. The length of the second operand is implicitly defined by the pattern. The pattern characters belong to these classes:

- SST substitution character (code 00100000);
- TSZ character of substitution and zero suppression termination (code 00100001);
- RSZ character of zero suppression start (code 00100010);
- INS insertion characters (any character different from the three previous ones).

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It must be remembered that the first character of the pattern is used during operation performance as "fill character".

The operation starts always in "zero suppression" conditions.

The instruction proceeds from left to right, examining the characters of the pattern.

Only when the examination of the pattern requires it, the decimal characters are considered, passing from one to the other.

The operation is performed in the following way:

1. - Zero suppression condition

If the pattern examination detects the presence of a SST character, the corresponding decimal character is examined. Should the numerical part of it be equal to zero, the pattern character is replaced by the fill character; in the opposite case (numerical part of the decimal number different from zero) the pattern character is substituted with the decimal character and the zero suppression condition is taken away.

In both conditions, the operation prepares itself to act on the following character of the field to be edited.

If a character TSZ is detected, the pattern character is always replaced with the decimal character, and the zero suppression condition is anyhow eliminated. If in the pattern a character RSZ or INS is detected, it commands the substitution with a fill character, without advancing the decimal field pointer.

2. - No zero suppression condition

The TSZ and SST characters both command the substitute operation, no matter what is the value of the corresponding decimal character. This last one therefore always replaces in the pattern field the TSZ or SST character, while the pointer of the field to be edited moves forward of one position.

The insertion characters are left unchanged in the pattern field, so that they show in the result. In this case, the pointer of the decimal field does not proceed.

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Also in this case, the pointer of the field to be edited does not proceed.

FAO4 FAO5

0	0	Not possible
0	1	Not possible
1	0	Operation ended in zero suppression condition
1	1	Operation ended in no zero suppression condition

5.5.3.7. Exclusive OR on Characters - XC

The instruction works bit by bit on the content of the two fields, performing the "exclusive or". The auxiliary character of the instruction indicates, with the usual rules, the length of two operands. The result is recorded at the place of the first operand, while the second stays unchanged. The operation proceeds from left to right, position by position.

FA04 FA05

0	0	Not possible
0	1	Not possible
1	0	Result equal to all zeroes
1	1	Result different from all zeroes

5.5.3.8. OR on Characters - OC

It operates as the previous one, with the only difference that it operates the "OR" operation.

Qualitative Result: it is not interested.

5.5.3.9. AND on Characters - NC

This instruction works, too, as the two previous ones, with the only difference that it performs an "AND" operation.

Qualitative Result: it is not interested.

5.5.4.

Research instruction

The format is a 2-address format:

OP	L	I1	I2
----	---	----	----

OP : type of operation

L : binary number representing the length of the research field, equal to L1+1 memory positions (from 1 to 256)

I1 : address of the research field, indexable or not.

I2 : address of the research field, indexable or not.

These instructions allow to search for, in a memory field, a pre-fixed character ("model"). The character position is determined storing, as a result of the operation, an address in the change register with number 7 (1111): the address is the one of the memory position following, in the direction of the research, the one of the first character found equal to the model.

In the case of research with negative result, the address stored is the one of the character following the end of the research field, in the direction of the research. The first address of the instruction always gives the research field, whose length is given, according to normal rules, by the auxiliary character.

The second address refers to the character to be searched (model).

Both the operands are unchanged.

5.5.4.1.

Search right - SR

This instruction searches in the first operand for a character equal to the second operand, proceeding from left to right. The operation stops as soon as it finds a character equal to the model, or at the end of the field. The address I1 is the one to the left.

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Qualitative Result:

FA04 FA05

0	0	Not possible
0	1	Not possible
1	0	Search with negative result
1	1	Search with positive result

5.5.4.2. Search Left - SL

It operates as the previous one, with the only difference that it examines the search field moving from right to left. The address I1 is the one to the right.

Qualitative Result:

FA04 FA05

0	0	Not possible
0	1	Not possible
1	0	Search with negative result
1	1	Search with positive result

5.5.5. Immediate instructions

There are in this group the instructions with two operands, one of which is specified in direct form by the auxiliary character of the instruction itself. The second operand is given through its address: its length is always of one character.

The format of these instructions is therefore the one with one address.

OP	K	I1
----	---	----

OP : type of operation

K : constant to be processed

I1 : address, indexable or not, of the memory character to be processed with K.

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5.5.5.1. Compare Immediate - CMI

The content K of the auxiliary character of the instruction, considered as a binary integer, is compared with the content of the storage position given by the address I1. The result is only qualitative.

Qualitative Result:

FA04 FA05

0	0	Not possible
0	1	The storage character is smaller than the K constant
1	0	The storage character is equal to the K constant
1	1	The storage character is greater than the K constant

5.5.5.2. Move Immediate - MVI

The constant K contained in the auxiliary character of the instruction is recorded in storage, in the position specified by the I1 address.

Qualitative Result: it is not interested.

5.5.6. Jump instructions

These instructions allow to interrupt the sequential performance of the program, in some cases conditioning the choice of the following instructions to the presence of certain conditions.

The instruction auxiliary character contains in its most significant half the jump "mask", i.e. a code indicating the conditions to be tested to decide whether or not to perform the jump. The less significant half of the auxiliary character must contain the 0000 code. The format is with one address:

OP	M	0000	I1
----	---	------	----

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OP : type of operation
 M : jump mask
 I1 : address, indexable or not, of jump destination

5.5.6.1. Jump on Condition - JC

The four bits of M give the couples of conditions of FA04 and FA05, which must be verified, in order to perform the jump.

If more than one bit of M is "1", the jump is performed when at least one of the corresponding conditions is verified.

The correspondence between the bits of M and the couples of values of FA04 and FA05 is:

	FA04	FA05
Bit 07	0	0
Bit 06	0	1
Bit 05	1	0
Bit 04	1	1

CM1 x, Alph
 alpha ex
 alpha x
 alpha x

Qualitative Result: it is tested but not altered.

Note: According to the given definition, if M = 0000, the jump never occurs; if M = 1111, the jump is unconditioned.

5.5.6.2. Jump Return - JRT

The four bits of M must be all at "1".

The instruction performs an unconditioned jump, which reserves at addresses 254 and 255 (Index register 7) the address of the subsequent instruction.

Qualitative Result: it is not interested.

Note: The JRT instruction described in para. 5.6.5.1. is a generalization of this one.

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5.5.6.3. Jumps on conditions - JS1, JS2, JIE

These instructions are similar to the JC; the meaning of the mask is though different, as it does not examine the Qualitative Result, but other conditions: the internal error and the operator panel keys. The following values of the M mask are allowed.

M = 1000 : jump on key 1 of operating panel (JS1)
 M = 0100 : jump on key 2 of operating panel (JS2)
 M = 0010 : jump on internal error, annulling the error condition (JIE)

Qualitative Result: it is not interested

Note: the third instruction is used for diagnostic purposes; normally it is not used because the internal error condition stops the Central Processor operations.

5.5.7. Various instructions

This group includes the instructions which allow to stop the computer, to condition its stopping, etc. None of these instructions modifies the qualitative. They all have formats without addresses.

OP	C
----	---

OP : type of operation
 C : binary configuration further specifying the type of operation.

5.5.7.1. Halt instruction - HLT

This instruction stops the machine and switches on the HALT light on the operator console. At the subsequent pressure of the START key, the machine starts again, performing the following instruction. The character C is not used and can have any value.

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5.5.7.2. No operation - NOP2

This instruction causes no operation.
The character C is not used, and can have any value.

5.5.7.3. Light On - LON

The performance of this instruction causes the switching on of the console light "Operator Call".
The character C must be 1000 0000.

5.5.7.4. Light Off - LOFF

The performance of this instruction causes the switching off of the console light "Operator call".
The character C must be 0100 0000.

5.5.7.5. Inhibit Stop - INS

This instruction inhibits the "Step-by-step" key. In this case the machine can be stopped only from the maintenance console, or from the program.
The character C must be equal to 0010 0000.

5.5.7.6. Enable Step - ENS

This instruction enables again the "Step-by-step" key, inhibited by the INS instruction.
The character C must be equal to 0001 0000.

5.6. Additional internal instructions

These instructions can be used only if the corresponding option is enabled.

5.6.1. Packed and signed decimal arithmetics

The additional decimal instructions operate on packed and signed data, and all of them have a 2-address format.

OP	L1	I2	I1	I2
----	----	----	----	----

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- OP : type of operation
 L1 : binary number indicating the length of the first operand, equal to L1+1 characters (from 1 to 16)
 L2 : binary number indicating the length of the second operand, equal to L2+1 characters (from 1 to 16)
 I1 : address of the rightmost byte of the first operand, indexable or not
 I2 : address of the rightmost byte of the second operand, indexable or not

Both the operands are located through the address of their less significant position (L1 and L2). The processing starts from the less significant position, considering the sign first and subsequently the numbers: the numbers are considered as integers and right aligned. The operands occupy a maximum of 16 storage positions each (corresponding to 31 decimal digits plus the sign). All the operations are performed algebraically: the addition, subtraction, comparison and transfer are done position by position, from right to left, while the multiplication and division take directly the second operand from storage before starting the operation, transferring it in a specialized storage zone. Such a zone, at the addresses 232 through 239 (hexadecimal 00E8 through 00EF) must not be used as operand, and is altered during operation. The operands with value zero and "minus" sign are used correctly; for the comparison they are equal to the ones with value zero and "plus" sign.

5.6.1.1. Add Packed - AP

The second operand is added to the first, and the obtained result is recorded in the field of this last one; the second operand stay unchanged. The sign of the result is the one of the first operand, should the signs of the two addends be equal or the absolute value of the first not be less than the second; in the opposite case, the sign is generated with one of the following configurations:

- C(1100) for the sign "+"
 D(1101) for the sign "-"

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The length L1 of the first operand must be greater or equal to L2; in the opposite case, an overflow signal is generated. This can occur also with $L1 \geq L2$, if the result cannot be contained in the field of the first operand.

Should L2 be less than L1, the necessary number of zeroes is added to the left of the second operand in order to perform the operation on all the length of the first operand.

In case of overflow, the result is uncomplete.

Qualitative Result:

FA04 FA05

0	0	Overflow
0	1	Result less than zero
1	0	Result equal to zero
1	1	Result greater than zero

5.6.1.2. Subtract Packed - SP

The second operand is subtracted from the first one, and the difference is recorded in the first operand field; the second operand stays unchanged. The operation proceeds in a way similar to the AP (and therefore the considerations made in the previous paragraph are still valid), with the exception for the processing of the sign, which is equal to the one of the first operand if the two operands have an opposite sign or if the first one has an absolute value not lower than the second one.

Qualitative Result:

FA04 FA05

0	0	Overflow
0	1	Result less than zero
1	0	Result equal to zero
1	1	Result greater than zero.

5.6.1.3. Multiply Packed - MP

The multiplication operation is performed; the first operand serves as multiplier, the second as multiplicand.

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The result thus obtained is recorded in the same field of the first operand which is therefore destroyed, while the second operand is not modified. The length of this last one should not be over eight positions (equal to 15 digits plus the sign) and must be less than the length of the multiplier.

In the opposite case, an overflow occurs. The multiplier must contain at least $L2+1$ characters to the left of numbers equal to zero, otherwise an overflow condition occurs. In case of overflow, the operation is not performed.

The multiplication is algebraic, and the sign of the result is generated in the standard configurations 1100 (+ sign) and 1101 (- sign), deducing it from the signs of the operands, according to the algebraic rules.

Qualitative Result:

FA04 FA05

0	0	Overflow
0	1	Result less than zero
1	0	Result equal to zero
1	1	Result greater than zero

5.6.1.4. Divide Packed - DP

The first operand is considered as dividend, the second as divider. The quotient and the remainder of the division are recorded in the dividend field: the quotient is placed leftmost ($L1 - L2$ positions) the remainder is placed rightmost ($L2+1$ positions). The divider stays unchanged.

In order not to have an overflow signal the following limits must be fulfilled:

- the length of the first operand must be greater than the one of the second operand ($L1 > L2$)
- the length of the divider must not be over eight positions ($L2 \leq 7$)
- the value of the operands must be such to allow the depositing of the quotient in the ($L1 - L2$) characters available
- the divider must be different from zero.

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In case of overflow, the operation is not performed. The sign of the remainder is equal to the one of the dividend; the sign of the quotient is generated according to the ones of the operands, according to the algebraic rules.

Qualitative Result:

FA04 FA05

0	0	Overflow
0	1	Result less than zero
1	0	Result equal to zero
1	1	Result greater than zero

5.6.1.5. Move Packed - MVP

The second operand is transferred in the field of the first operand. If the field to be transferred has a length below the one of the destination field, the operand is completed to the left with not significant zeroes. An overflow indication occurs, if the condition $L1 < L2$ occurs. In this case the operation is performed, but it generates an incomplete result. The sign of the result is coincident with the one of the starting field; this last one stays unchanged.

Qualitative Result:

FA04 FA05

0	0	Overflow
0	1	Operand lower than zero
1	0	Operand equal to zero
1	1	Operand greater than zero

5.6.1.6. Compare Packed - CMP

The two operands, not being altered, are compared algebraically; the result of the operation is only qualitative. For this comparison a positive zero and a negative zero are considered equal. It must be noted that the operation proceeds regularly no matter how the operands fields are arranged.

An overflow indication occurs, when $L1 < L2$.

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Qualitative Results:

FA04 FA05

0	0	Overflow
0	1	First operand smaller than the second
1	0	First operand equal to the second
1	1	First operand greater than the second

5.6.2.

Format conversion instructions

In this group there are the instructions for packing and expanding signed data, which transform unpacked numerical operands in packed operands and viceversa.

The instructions of this type have 2 addresses:

OP	L1	L2	I1	I2
----	----	----	----	----

OP : type of operation

L1 : binary number defining the length of the first operand, equal to L1+1 characters (from 1 to 16 words)

L2 : binary number defining the length of the second operand, equal to L2+1 characters (from 1 to 16 words)

I1 : address of the rightmost byte of the first operand, indexable or not

I2 : address of the rightmost byte of the second operand, indexable or not

The operands are located through the address of their rightmost position, and the operations proceed from right to left.

5.6.2.1.

Pack with Sign - PKS

The second operand, considered as unpacked, is transferred in the field of the first one, giving it a packed and signed format. The operation goes on writing the result word as soon as the sufficient information is read from the second operand.

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Should $L2 < 2L1$, the first operand is completed to the left with non significant zeroes: If, to the contrary, $L2$ is greater than $2L1$ the left digits of the second operand, which cannot be located in the field of the first operand, are ignored.

The packing interprets the combination 1010 in the "zone" of the first character to the right of the first operand as a "-" sign and any other combination as a "+" sign. According to this rule it generates the sign of the packed result, fixing for the "+" sign the configuration 1100 and for the "-" sign the configuration 1101.

Qualitative result:

FA04 FA05

0	0	Not possible
0	1	Result less than zero
1	0	Result equal to zero
1	1	Result more than zero

5.6.2.2. Unpack with Sign - UPKS

The second operand, decimal, packed and signed is trasfer red in the field of the first one, giving it an unpacked format.

For every result word to be generated only the information strictly required by the second operand is read; the result is then stored, and the reading of the second operand starts again.

The second operand is a decimal field of $(L2+1)$ positions which, therefore, contains $(2L2+1)$ digits plus the sign. For this reason, if $L1$ is greater than $2L2$, the first operand is completed to the left with meaningless zeroes. If instead the $L1$ portion is smaller than $2L2$, those digits to the left of the first operand, that do not find place in the field of the first operand, are ignored.

The unpacking always generates the 0100 zone, on all the digits, only leaving, in the qualitative, the information dealing with the sign and the value of the packed operand.

Qualitative Result:

PA04 PA05

0	0	Not possible
0	1	Decimal operand less than zero
1	0	Decimal operand equal to zero
1	1	Decimal operand more than zero

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5.6.3. Logical Instructions of Immediate type

They are a complement to the instruction group of the type constant-memory of the basic mode and therefore present similar characteristics. They have a one address format. Of the two operands one is specified directly by the auxiliary character of the instruction, and the other is detected by the address.

OP	K	I1
----	---	----

OP : type of operation
 K : constant to be operated
 I1 : address, indexable or not, of the memory character to be operated with K.

5.6.3.1. OR Immediate - OI

The OR between the constant K and the memory character addressed by I1 is performed bit by bit. The result is recorded in memory in the I1 position.

Qualitative Result: it is not interested.

5.6.3.2. AND Immediate - NI

The instruction works as the previous one, with the only difference that it performs an "AND".

Qualitative Result: it is not interested.

5.6.3.3. Exclusive OR Immediate - XI

It works as the previous ones, performing, though, the the "exclusive OR" operation.

Qualitative Result:

FA04 FA05

0	0	Not possible
0	1	Not possible
1	0	Result equal to zero
1	1	Result different from zero

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5.6.3.4. Test under Mask - TM

The instruction is completely similar to the NI, with the only difference that the result is not written in memory, and the qualitative result is modified. The instruction is used to test the value of some bits of a word, signaling the case when some of those detected by the "1" of the K mask have a "1" value.

Qualitative Result:

FA04 FA05

0	0	Not possible
0	1	Not possible
1	0	Result equal to zero
1	1	Result different from zero

5.6.4. Operations on Index Registers

This group of instructions is used to operate directly on the Index Registers. They all have a 1 address format, and operate for lengths equal to 2 characters.

OP	1	N	0000	I1
----	---	---	------	----

OP : type of operation

N : number of the index register, variable from 000 to 111, on which to operate

I1 : address, indexable or not, of the rightmost byte of the second operand.

All the operations proceed word by word, from right to left.

5.6.4.1. Load Register - LD

The content of the memory field, addressed by I1, is transferred to the N index register.

Qualitative Result: it is not interested.

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5.6.4.2. Add Memory to Register - AMR

The content of the memory field, addressed by I1, is added to the content of the N index register, and the result is recorded in this last register. The operation is performed considering the two operands as binary integers, and losing any possible carry over beyond the length of 16 bits (overflow).

Qualitative Result:

FA04 FA05

0	0	Result equal to zero
0	1	Result different from zero
1	0	Overflow and partial result equal to zero
1	1	Overflow and partial result different from zero

5.6.4.3. Subtract Memory from Register - SMR

It works as the previous one, with the only difference that a subtraction is performed and the result is left in form complemented to 2¹⁶.

Qualitative Result:

FA04 FA05

0	0	Not possible
0	1	Result smaller than zero (complemented)
1	0	Result equal to zero
1	1	Result greater than zero

5.6.4.4. Compare Memory to Register - CMR

The content of the N register is compared with the memory field at address I1; the operation gives a purely qualitative result, without altering the memory field nor the index register.

Qualitative Result:

FA04 FA05

0	0	Not possible
0	1	Register smaller than memory
1	0	Register equal to memory
1	1	Register greater than memory

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5.6.4.5. Store Register - STR

The content of the N register is transferred to the memory field with address I1.

Qualitative Result: it is not interested.

5.6.4.6. Load Address - LA

The address I1 specified in the instruction is stored in the N register, after it has been modified by possible indexing operations.

Qualitative Result: it is not interested.

5.6.5. Jump instructions5.6.5.1. Jump Return - JRT

This instruction is a generalization of the one of the basic set of instructions (refer to 5.5.6.2.) in which the use of values of M other than 1111 is allowed.

It tests the various configurations of the qualitative exactly as the JC instructions (refer to 5.5.6.1.) and it jumps only in case of checked condition.

It though deposits unconditionally the address of the subsequent instruction in register 7.

In particular, the instruction M = 0000 never performs the jump and it limits itself to the reservation of the address of the subsequent instruction in register 7, before performing it.

5.6.5.2. Load Program Status Register - LPSR

This instruction has the following format:

OP	C	I1
----	---	----

OP : type of operation

C : not used character, with any value

I1 : address, indexable or not, of the leftmost byte of the operand.

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The operand consists of 4 words, and its content is used to load the program status register (refer to 5.1. and 5.2.).

The bits of the first word are used in the following way:

05 : to load FA04
04 : to load FA05
00 : to load FA06, interruption mask

The second word is ignored, as for the other bits of the first word.

The last two words are used to load the program address er.

Qualitative Result: FA04 and FA05 are loaded with new values, as given in the previous description.

5.6.6. Diagnostic instruction - LOLL

The auxiliary character C must be equal to 1000 0001. This instruction must be used only during diagnostic performance. Its effect is the one of increasing the cycle period of the Central Processor; it must be kept in mind that the operations, implying data transfer with peripherals, must occur always with a nominal cycle period.

The increase in the machine cycle stops with a normal LOFF instruction or by pressing the CLEAR push-button on the panel. The LOLL instruction switches on also the panel bit lamp "OPER.CALL".

5.7. Compatibility with the 115/1 and 115/2

Here below there is a list of the possible situations in which the fact of not complying with the limits (already indicated in the manuals) might cause the incompatibility of the programs with the 115/1 and 115/2, at the internal instructions level.

- Use of undefined operation codes.
- Use of C characters different from the ones defined, when there are some limits (jump instructions, various instructions).

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COMPIL.	/cb	APP. <i>for</i>	SEC. S.P.S. - GEISI	N° 30004122 o/a	
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- Use of invalid addresses, or application of the memory circularity. (In particular, it must be noted the case of the instructions SR, SL, JRT which interest the fields at the margins of memory.)

The programs complying with the rules mentioned work on the GE 130 as on the previous machines.

A further incompatibility could be raised using a block above 129 characters for the program loading.

5.8. External operations

5.8.1. General

There is a single external instruction (symbolic code PER) which allows to perform all the external operations given below.

The PER instruction allows an alternative (symbolic code PERI), in which the name of the peripheral unit to be selected is indicated in an indirect way. The external operations which can be programmed with the external instruction are:

- a) TPER - Data Transfer Start from or to Peripheral Unit
- b) CPER - Command sent to Peripheral Unit
- c) EPER - Test Peripheral Unit condition
- d) SPER - Unload conditions of Channel 3.
- e) LPER - Test availability of Channel, Connector and Peripheral Unit.

The C.P.U., during the program performance, starts in sequence the external operations: they can afterwards continue autonomously, while the C.P.U. carries on with the program.

If the operation started is a character transfer, the program performance is always delayed and in certain cases completely interrupted.

When the Peripheral Units are performing certain operations, they are not in the condition of accepting the command to start some others, and send a signal of unit "busy" or "not available" (PEOO).

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The performance on an operation on a peripheral unit of a multiple controller may or may not use the controller: in the first case all the peripheral units connected with the controller are "not available" (e.g.: tapes controller in reading or recording); in the second case the other peripheral units of the controller are not influenced and can be "available" or "free" (e.g.: tape unit in re-wind).

When data transfers occur in overlapping, the program may meet an external instruction in one of the following situations:

- the channel selected by the instruction is busy for a transfer;
- the selected peripheral unit, or another unit of the same controller, or another controller connected (through a MultiPeripheral Adapter) to the same connector, are busy in a transfer.

These conditions, which forbid to perform the instructions TPER, CPER, EPER, SPER are called "channel" or "connector" busy.

A situation of the peripheral units will be given further on and a division will be made between "unavailability" and "out-of-service", in which because of an electric failure, or a mechanical inconvenience or the lack of voltages, the peripheral unit cannot perform correctly (and can be obliged to end irregularly) some operations. A third situation, separate from the other two, is the one of peripheral units in "manual", or "STAND BY": this situation occurs when an operator intervention is required on the peripheral unit before the unit itself can continue the operations. The opposite situation, reset by the operator intervention, is called "automatic" or "OPERATE". The only relationship between the above mentioned conditions is the following: when an "out-of-service" occurs, it always makes the peripheral unit, the connector and the channel "available", and set the peripheral unit in "manual".

In normal conditions, a peripheral unit can switch to "manual" while it is "not available" and ends regularly the operation started, before being available to the operator.

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5.8.2.

External instruction - PER/PERI

Format:

OP	C	I1
----	---	----

OP : type of operation

C : auxiliary character

I1 : address, indexable or not, of the leftmost byte of the memory zone which defines more the operation to be performed.

OP - Type of operation

Distinguishes PER from PERI and from the other instructions.

C - Auxiliary character

In the case of PER it is the name of the peripheral unit to be selected.

In the case of PERI it is any character, not used.

In this case, the name of the peripheral unit to be selected is taken from the memory word at the address 224 (hexadecimal 00E0).

I1 - Address

"I1" addresses the first one of a group of characters (6 for the TPER and 2 for the other instructions), which specify completely the operation to be performed:

TPER :	Z	X	L	L	I	I
--------	---	---	---	---	---	---

I1

CPER, EPER, SPER, LPER :

Z	X
---	---

I1

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The Z character specifies the type of operation, some procedures to perform the operation itself, and the interested channel.

The X character further specifies an operation, among the ones of a certain type.

The fields LL, II specify, in the case of TPER, the length and the address of the memory area interested to the transfer of data with the peripheral unit.

For further details refer to the following description.

5.8.3. Description of the external instruction

5.8.3.1. Elements common to all types of operations

- The bits 03 and 00 of the Z character indicate the channel to be used, according the following code:

03	00
0	0
1	0
0	1
1	1

Channel 1

Channel 3

Channel 2 not overlapped
to calculation

Channel 2 overlapped to
calculation

- The distinction between two types of utilization of the channel 2 is meaningful only for the TPER instruction and refers to the performance of the transfer to be started.
- The indication of the channel must be coherent with the one of the peripheral unit selected: channel 2 is reserved to the integrated parallel printer and reader; channels 1 and 3 cannot be used with the integrated parallel printer.
- If the selected channel or connector are busy, a TPER or CPER, EPER, SPER instruction cannot be performed immediately.

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An automatic recycle is then done on an external instruction to generate a waiting period to phase-in the execution. This waiting period can be stopped by the occurrence of an enabled interruption.

An LFER instruction, only issued to test the channel or connector busy condition, is not stopped by this condition.

- The bit 02 of the character Z is used to require a preliminary analysis of the availability of the selected peripheral unit.
If the bit value is "1", the status of the peripheral unit is ignored and the instruction is performed without taking it into account.
If the bit value is "0", the instructions TPER, CPER, EPER block the C.P.U. in a waiting period similar to the one described above, until the unit is again available; the instruction LPER takes into account, in the generated qualitative, the availability of the peripheral unit, beside the availability of the channel and the connector.

5.8.4. TPER: Start data transfer from or to peripheral unit

5.8.4.1. Start

- A command is sent to the interested peripheral unit, in order to start the transfer of a certain number of characters from memory to an external medium or vice-versa, after the possible period of waiting due to channel or connector busy or peripheral unit not available.
- It clears the indicator of "parity error in input" on the interested channel.
- A control on the acceptability of the command is performed by certain controllers with standard interface.
The result of this control is available for the program in the qualitative.
The real transfer only starts if the command has been accepted. In the opposite case, the interruption ends with no characters exchange.

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- If the transfer is in overlap (Channel 2 overlapped or Channel 3) the instruction ends when the transfer starts, and the program performance continues while the transfer is going on.
If the transfer is not overlapped, the last character must be exchanged before passing to the following instruction.

5.8.4.2. Performance

- The transfer consists of the exchange of characters between C.P.U. and peripheral unit. In output the characters are read from memory and sent to the peripheral unit. In input, the characters sent from the peripheral unit are written in memory. The memory is then examined according to increasing or decreasing addresses, starting with the address (II) specified by the TPER operand.
- During the transfer in input, the C.P.U. performs an odd parity check on the characters received from peripheral unit (with the exception of the integrated reader), and causes, in the negative case, the "parity error in input" condition on the interested channel. This check is done also on the photodisc codes, received by the integrated printer during printing. The check is normally corrected before storing the data in memory.
- The controller and the peripheral unit interested to the transfer are then "occupied" and can stay in this condition for a certain period of time after the exchange of the last character (which to the contrary makes channel and connector "available"). During this period the operation is completed (e.g. : end of the performance of certain controls), or actually performed (e.g.: printing of the printer with buffer).

5.8.4.3. End

- The end of the transfer occurs when at least one of the following conditions is present:

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- a) the length (LL + 1) specified in the instruction has been occupied;
- b) the peripheral unit sends a signal of "end" (e.g.: end of block during tape reading),
- c) the peripheral unit switches to "out-of-service";
- d) the transfer on channel 1 interests one of the Datanets (working on connector 4) which sends the "permission to disconnect" while the channel 2 is not busy.

On channel 2 there is not the distinction between ends "a" and "b" in the qualitative result.

- The transfer gives a certain number of auxiliary information, accessible by the program for subsequent processing:

- e) address subsequent to the one of the last character exchanged, in the chosen scanning direction of memory;
- f) reception of the "end" signal from peripheral unit (refer to point "b" above) simultaneous or not to another one of the end causes;
- g) parity error in input.

On channel 1, the information "e" is directly unloaded in register 7 and the information "f" in the qualitative result, at the end of the operation, before performing the following instruction.

The information "g" can be tested later with an EPER instruction.

On channel 2, the information "e" and "f" are not generated, and "g" can be tested with an EPER instruction. On channel 3, the three information stay, at the end of the transfer, in the machine registers and can be unloaded with the SPER instruction.

After the SPER instruction, they are accessible as if the operation was performed on channel 1 (i.e. they are set respectively in register 7, in the qualitative result, and in the indicator of "parity error in input" of channel 1).

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5.8.4.4. Overlappings

- One TPER on channel 1 make always the C.P.U. wait for the exchange of the last character, before switching to the next instruction.
If the TPER on channel 1 has been immediately preceded in the program by a TPER on channel 2, of the "overlapped" type, the calculation starts again only when both transfers have been completed; this period of waiting has been included because of compatibility with the 115-1 and 2.
- One TPER on channel 2 can start a transfer both in an overlapped mode and in a not overlapped mode. This last possibility has been planned only for compatibility with the 115-1 and 2, as, after having started an overlapped operation on channel 1, any following EPER instruction concerning the same channel and peripheral unit is enough to cause the waiting for the end of the operation.
- A TPER on channel 3 starts always a transfer in overlapping. After having performed it, and before performing any other instruction concerning the same channel (LPER excepted), the channel must be unloaded with a SPER instruction which waits for the end of the transfer (if this is not yet over) and makes the associated auxiliary information available.
Any other instruction referring to channel 3 would cause the loss of the auxiliary information.

5.8.4.5. Input with packing on channel 1

A command can be given on channel 1 for an input with packing. During this operation, every character received from peripheral unit is treated in the following way: its 4 most significant bits are eliminated and the 4 less significant bits of the two subsequent characters are packed to form a character to be recorded in memory (the first character contributes to form the 4 most significant bits; the second the other 4).
If the peripheral unit interrupts the transfer after the reception of an odd number of characters, the last character is recorded in memory as it has been received.

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The end on length from the Central Processor is issued when the 2(LL+1)th character is received from peripheral, when the packed (LL+1)th memory character is completed.

5.8.4.6. Specialized Datanet connection

Because of the compatibility with the 115-1 and 2, the possibility to use on connector 4 the "permission to disconnect" of the Datanets has been provided. When a transfer on channel 1 is performed through a Datanet connected on connector 4, the transfer can be ended in a special way.

Some Datanets have in fact the possibility to store in a buffer a certain number of characters transferred on line; this allows the C.P.U. to disconnect itself for a short period of time from the Datanets, while the buffer is filled (during reception) or when is emptied (during transmission).

The condition of "buffer full in reception" or "buffer empty in transmission" is signaled by the C.P.U. as "permission to disconnect itself" from transfer, and causes the end of the transfer if the channel 2 is not busy.

The C.P.U. is in this case disconnected from the Datanet connection, and has a certain period of time to perform some operations, before being connected again through a TPER instruction.

The new TPER will have to specify, as initial address (II), the one stored in register 7 at the end of the previous transfer phase.

The C.P.U. can make a distinction of this situation from the one of normal end of transfer examining the qualitative result and the memory address reached.

The C.P.U. will have also to examine, before being connected again, whether the previous transfer has determined an indication of "parity error in input", which would be destroyed by the new TPER.

5.8.4.7. Format of the operand

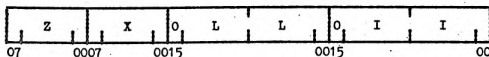
The operand of an external instruction of the type TPER has the following format:

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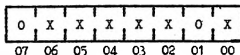
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- Z character



The meaning of the bits 03, 00 is given in 5.8.3.1.
 The bit 02 is normally set to "0", to wait for the peripheral unit available.
 The other bits indicate:

- Bit 06 0 Transfer in input
 1 Transfer in output
- Bit 05 0 Memory scanning for increasing addresses
 1 Memory scanning for decreasing addresses
- Bit 04 0 Input with packing
 1 Input without packing or output

The input with packing is possible only on channel 1 and cannot be overlapped with other external data transfer operations.
 On channel 2 only the printing operations on an integrated parallel printer and the reading operations on an integrated reader can be performed.

- X character

It has been sent to the peripheral unit, which interprets it as a command.

The list of the commands recognized by the various peripheral units is mentioned in the manuals of the units themselves.

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- LL and II characters

The LL characters indicate in binary the length of the transfer, minus 1. The exchange of data interests always a number of words not above (LL+1); such a limit may also not be reached if the operation ends before, for reasons different from the length end.

The II characters indicate the address, in an unindex able form, of the first memory word interested to the transfer.

On channels 1 and 3, II may have any value, provided it is valid; LL may have any value, provided the defi ned memory field stays all in valid addresses.

On channel 2, LL and II have some limitations, accord ing on the integrated peripheral used:

a) Integrated parallel printer

The TPER is driven with Z = 0101 X001 (hexadecimal 59 or 51), which means "output for increasing addresses, waiting, on channel 2".

It must be II = K.256+2, with K = 0, 1, 2, ...

LL = 159

Note: The printing occurs always on the number of columns actually assembled on the printer, but the analysis of memory may interest an higher number of characters, up to a maximum of 160.

For the compatibility between machines having a different number of columns of print it is advisable that the areas of print used be always of 160 characters, and the possible unused part to the right be filled in with "blank" characters (x, hexadecimal 50).

The value LL = 159 is coherent with this approach, but in reality LL is not used.

The two characters to the left of the print area (addresses K.256 and K.256+1) are used to check the print, and their content is destroyed (i.e. brought to an undefined value) by the execution of the print.

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b) Integrated card reader

The TPER on channel 2 is driven, with $Z = 0001\ X001$ (hexadecimal 19 or 11), which means "input for increasing addresses, waiting, on channel 2".
It must be $II = K.256+2$ with $K = 0, 1, 2, \dots$

$LL = \begin{cases} - 79 & \text{for normal reading} \\ - 159 & \text{for binary or mixed reading} \end{cases}$

Note: The given value of LL is coherent with the fact that the reading interests always a whole card, but in reality LL is not used.

c) Integrated document reader

The TPER on channel 2 is driven with $Z = 0011\ X001$ (hexadecimal 39 or 31), which means "input for decreasing addresses, waiting, on channel 2".

It must be $II = K.256+N+1$ with $K = 0, 1, 2, \dots$
 $LL = N-1$

if $N (\leq 256)$ is the maximum number of characters on the documents read.

Note: Refer to the notes sub previous point "b".

5.8.4.8. Qualitative result and auxiliary informationa) TPER on channel 1

FA04 FA05

0	0	Command not accepted, operation not performed
0	1	Not possible
1	0	Operation performed, and terminated without "end" from peripheral unit
1	1	Operation performed, and terminated with end from peripheral unit.

- The answer "command not accepted" is issued only by certain controllers with standard interface.
- The operation unloads in register 7 the address subsequent to the one of the last character exchanged, in the direction of the memory scanning fixed by the bit 05 of Z.

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b) TPER on channel 2

- It leaves always FA04 = 1, FA05 = 0 and does not issue any other information. The command is always accepted.

c) TPER on channel 3

FA04	FA05	
0	0	Command not accepted, operation not performed
0	1	Not possible
1	0	Operation started
1	1	Not possible

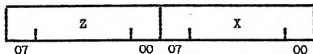
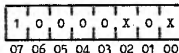
5.8.5. CPER - Send command to peripheral unit5.8.5.1. Performance

- After a possible period of waiting, a command is issued to the interested peripheral unit.
- It clears the indicator of "parity error in input" of the interested channel.
- A control on the acceptability of the command is done by certain controllers with standard interface. The performance of the command occurs only if the command has been accepted. The result of this control can be addressed with an instruction EPER.
- The instruction ends with the acceptance of the command from the peripheral unit. In certain cases the command performance is thus over. In others, the performance of the command employs the peripheral unit (with or without the related controller) for a certain period of time, while the C.P.U. goes on with the program. The peripheral unit sends then the signal of "unavailability".

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5.8.5.2. Format of the operand

The operand of an external instruction of the type CPER has the format:

- Z character

The meaning of the bits 03, 00 is given in 5.8.3.1. The issue of a command is significant only on channel 1 and 2 (not overlapped), therefore the 03 bit is always equal to "0".

Bit 02 is normally set on "0", to ask to wait for peripheral unit available.

An exception is made for those peripherals which are able to perform several independent operations (e.g.: a printer with double paper trailer declares itself "not available" if there is a paper movement on the first trailer, in order to stop a possible printing instruction; in these conditions, it can though accept regularly a paper movement command on the second trailer, which is issued setting on "1" the bit 02 of Z).

- X character

It is sent by the peripheral unit, which interprets it as a command. The list of commands recognized by the different peripheral units is given on the manuals of the units themselves.

The command must be coherent with the character Z preceding it, i.e. it must not mean, for the peripheral unit, the beginning of a transfer.

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5.8.5.3. Qualitative Result

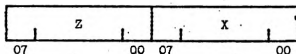
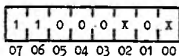
It is always FA04 = 1, FA05 = 0.

5.8.6. EPER - Check the peripheral unit condition5.8.6.1. Performance

- It examines, after a possible period of waiting, a condition related with the interested peripheral unit. The result of the exam is given as a qualitative result.
- Every peripheral unit sends a certain number of signals, useful to the program to check its operations. Some of the signals have a standardized meaning: they are the ones of "availability", "out-of-service", "manual", "command not accepted", "channel error", "external error". The other signals have a variable meaning depending on the type of peripheral unit.

5.8.6.2. Format of the operand

The operand of an external instruction of the EPER type has the format:

- Z character

The meaning of the bits 03, 00 is given in 5.8.3.1. The checking of the condition is possible only on channel 1 and 2 (not overlapped), therefore the bit 03 is always equal to "0".

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The parity error in input on channel 3 must be transferred, with a SPER instruction, on the one of channel 1, in order to test it.

The bit 02 may have a "0" or a "1" value: it must be set to "0", specifying "wait" for peripheral unit available if the addressed peripheral unit has an operation under way, and if the condition to be examined can be addressed only at the end of the operation (e.g.: the check of the recording on tape, which issues the signal "external error", ends only when the unit is again "available" after a recording).

- X character

It specifies the condition to be addressed. Certain values of X test only one condition. Others perform the check if there is at least one out of a certain group of conditions.

For further details refer to the Table of the values of X enclosed, and to the various manuals of the peripheral units.

5.8.6.3. Qualitative result

FA04	FA05	
0	0	Not possible
0	1	Not possible
1	0	Condition absent
1	1	Condition present

5.8.7. SPER - Unloading of the channel conditions

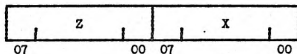
5.8.7.1. Performance

- The instruction, after a possible period of waiting, unloads the auxiliary information concerning the last transfer performed on channel 3, making them addressable by the program.

5.8.7.2. Format of the operand

The operand of an external instruction of the SPER type has the format:

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- Z character

It has the fixed value 1100 1100 (hexadecimal CC).

- X character

It has the fixed value 0100 0000 (hexadecimal 40).

5.8.7.3. Qualitative result and auxiliary information

FA04	FA05	
0	0	Not possible
0	1	Not possible.
1	0	Operation terminated without the "end" from peripheral unit
1	1	Operation terminated with the "end" from peripheral unit

- The operation unloads in register 7 the address subsequent to the one of the last character exchanged (on channel 3), in the scanning direction of memory.

- The condition of "parity error in input" of channel 3 is transferred in the corresponding indicator of channel 1.

Note the analogy with the final conditions of the TPER on channel 1.

5.8.8. LPER - Test the availability of the channel, connector, and peripheral unit5.8.8.1. Performance

- The instruction is used to test whether a transfer operation, started in overlapping, is over or not, avoiding the block that the other instructions undergo when they are issued with channel or connector busy. The instruction examines the conditions of channel and connector busy, of peripheral unit availability and issues a qualitative result.

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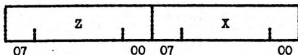
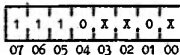
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5.8.8.2. Format of the operand

The operand of an external instruction of the LPER type has the format:

- Z character

The meaning of the bits 03, 00 is given in 5.8.3.1. A LPER on channel 1 (which, as it does not work in overlapped, can never give the busy signal to the C.P.U.) can be used to test the condition of connector busy, independently from the channel. Bit 02 may have a value "0" or "1".

In the first case, also the peripheral unit contributes to determine the answer "operation under way".

In the second case, a possible condition of "unavailability" of the peripheral unit is ignored.

- X character

It has the fixed value 0000 0000.

5.8.8.3. Qualitative Result

FA04	FA05	
0	0	Not possible
0	1	Not possible
1	0	No operation under way
1	1	Operation under way

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5.9.

Compatibility with the 115/1 and 115/2

The described external instruction includes the same performances which are present in the instruction of the 115/1 and 115/2 (*).

In particular, the 115/1 and 115/2:

- allow the indication of "Channel 3" in the TPER;
- after a TPER overlapped on channel 2, always perform another one on channel 1, immediately subsequent in the program;
- cannot perform the instructions SPER, LPER and the alternative PERI.

The compatibility is ensured in the sense that the programs of the 115/1 and 115/2 written comply with all the rules given in the manuals, and can work in the same way on the GE 130.

- (*) Note: The 115/1 and 115/2 are different one from the other for some details, as far as the behavior in case of command rejection and the addressable external conditions are concerned.
The GE 130, in these situations, behaves as the 115/2 (P.P.S. No. 300740450).

5.10.

Summary tables

5.10.1.

Values of the Z character

The values are all hexadecimal.

The first column gives the values which cause the testing of the Peripheral Unit availability; the second the values which avoid it.

An asterisk distinguishes the operations which are possible on the 115/1 and 115/2.

The values in square brackets are possible, but they are not useful for any peripheral unit existing at present.

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1) Integrated parallel printer (channel 2)

* TPER with overlapping (printing)	59	-
* TPER without overlapping (printing)	51	-
* CPER	81	85 (1)
* EPER	C1	C5
LPER	E1	E5

2) Integrated card reader, used on channel 2

* TPER with overlapping (forward reading)	19	-
* TPER without overlapping (forward reading)	11	-
* CPER	81	-
* EPER	C1	C5
LPER	E1	E5

3) Integrated document reader, used on channel 2 (2)

* TPER with overlapping (reverse reading)	39	-
* TPER without overlapping (reverse reading)	31	-
* CPER	81	-
* EPER	C1	C5
LPER	E1	E5

4) Operations on channel 1

(Standard controllers, integrated reader, serial printer on connector 1) (3)

* TPER forward reading with packing	00	[04]
* TPER reverse reading with packing	20	[24]
* TPER forward reading	10	[14]
* TPER reverse reading	30	[34]
* TPER forward recording	50	[54]
* TPER reverse recording	70	[74]
* CPER	80	84
* EPER	C0	C4
LPER	E0	E4

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5) Operations on channel 3

(Standard controllers, integrated reader, serial printer on connector 1) (3)

TPER forward reading	18 [1c]
TPER reverse reading	38 [3c]
TPER forward recording	58 [5c]
TPER reverse recording	78 [7c]
SPER	- CC
LPER	E8 EC

Notes:

- (1) Used only for the commands of the second trailer
- (2) Performance planned, but at present not used
- (3) For a given peripheral unit, normally only a part of the specified operations is significant.

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5.10.2. Qualitative resultsa) Internal instructions

		FA04 (OF)		FA05 (NZ)	
		0,0	0,1	1,0	1,1
TM	-	-	-	Result = 0	Result \neq 0
CMi	-	-	Storage < K	Storage = K	Storage > K
XI	-	-	-	Result = 0	Result \neq 0
CMR	-	-	Reg. < Storage	Reg. = Storage	Reg. > Storage
AMR	Result = 0	-	Result \neq 0	Result = 0 and OV	Result \neq 0 and OV
SMR	-	-	Result < 0	Result = 0	Result > 0
CMC	-	-	OP1 < OP2	OP1 = OP2	OP1 > OP2
XC	-	-	-	Result = 0	Result \neq 0
SR	-	-	-	Negative result	Positive result
SL	-	-	-	Negative result	Positive result
EDT	-	-	-	Termination in suppression	Termination not in suppression
MVP	OV.	-	Result < 0	Result = 0	Result > 0
CMF	OV.	-	OP1 < OP2	OP1 = OP2	OP1 > OP2
AP	OV.	-	Result < 0	Result = 0	Result > 0
SP	OV.	-	Result < 0	Result = 0	Result > 0
MP	OV.	-	Result < 0	Result = 0	Result > 0
DP	OV.	-	Result < 0	Result = 0	Result > 0
PKS	-	-	Result < 0	Result = 0	Result > 0
UPKS	-	-	Result < 0	Result = 0	Result > 0
MVQ	Result = 0	-	Result \neq 0	-	-
CMQ	-	-	OP1 < OP2	OP1 = OP2	OP1 > OP2
AD	Result = 0	-	Result \neq 0	Result = 0 and OV	Result \neq 0 and OV
SD	-	-	Result < 0	Result = 0	Result > 0
AB	Result = 0	-	Result \neq 0	Result = 0 and OV	Result \neq 0 and OV
SB	-	-	Result < 0	Result = 0	Result > 0

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b) PER - PERI external instruction

FA04 (OF) , FA05 (NZ)				
	0,0	0,1	1,0	1,1
TPER Chan.1	Rejected command	-	Termination with out external Terminate	Termination with external Terminate
TPER Chan.2	-	-	(always)	-
TPER Chan.3	Rejected command	-	Operation started	-
CPER	-	-	(always)	-
EPER	-	-	Condition absent	Condition present
SPER	-	-	Termination with out external Terminate	Termination with external Terminate
LPER	-	-	No operation under way	Operation under way

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6. DETAILED DESCRIPTION OF THE INTERNAL LOGIC6.1. Signal names

The machine signals have names of 4 characters plus an ending.

The positive going signals have a numerical ending (1, 2, 3, 4, etc.).

The negative going signals have an alphabetical ending (A, B, C, D, etc.), refer to the example of the following page (figure 4).

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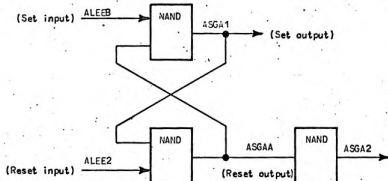


Fig. 4 - Signal name example

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6.2. Signals location

- The location of the most important signals is given during the description in the block logic drawing.
- The indication may be in parentheses.
Before the number of the chapter then the number of the interested box is given.
- In the case of the FF an indication is given only for one of the boxes forming the FF itself.
- The topographic location can be inexact as a consequence of the changes.
In case of discrepancies, it is necessary to refer to the general index of the signals.

6.3. Interpretation of the instructions

The program performance consists of the reading, recognition and subsequent performance of the elementary instructions recorded in memory.

The performance of a general instruction takes place in two phases:

- a) phase α : this phase reads from memory the characters forming the instruction with which the parts of the unit interested to the effective performance of the instruction are set;
- b) phase β : the operations required for the performance of the instruction are done during this phase.

The performances of phases α and β is done performing with a suitable sequence a determined number of "states".

For status we intend a special configuration present at the input of the sequential logic network of the sequence logic matrix (MLS).

The course or sequence of the states required to perform phase α and β is described in the specific documentation. (Flow charts code 14023130).

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It is set in the E6 status of phase α of the jump instructions (CI38) only if the signal DC16 ("verified condition") is present.

- FF ARES (022-4); it allows the loading of S0 during the first one of the states 0/0 which are performed after starting the timing through the "Clear" switch. The configuration that is loaded is 8/0 (refer to forcing status 14023130 fig. 6).
The status 8/0 is the first one that is performed when "Start" is pressed after having pressed "Clear".
It is set pressing "Clear".
It is reset with the TI10 pulse concerning the first status 0/0 which is performed.
- FF ADIR (024-2); it disables the function of the "Step-by-Step" key.
It is set with the CI77 issued by the INS instruction.
It is reset with the CI78 issued by the ENS instruction or with "Clear".
- FF ACIC (022-14); it is the FF of recycle of the Delay Line.
Initially it is set by "Clear".
After that it is set and reset cyclicly.
The reset pulse is the TO10, the normal setting pulse is the TO90 if a LOLL instruction has not been performed (PODIB=1 022-23).
In this case it is set by the TI05 with a delay of about 130 ns.
- FF ASTO (025-15) enables the recycle of the Delay Line if there are no stop conditions in timing.
In fact, this FF is reset with the OR of the following conditions: insertion of switch PATE or presence of internal error or inexistent address.
These last two reset ASTO only if the INAR switch is not inserted.
- FF ALTO (025-15) if set it stops the performance of the internal processing cycles (while the timing continues to cycle).
It is reset when "Start" is pressed and released.

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The possible set conditions are:

- AORE3=1 (025-13) signal arriving from the effective work timer (VAR 360), when the "Stand By" key is pressed.
- CAGU7=1 (025-13) this signal is the OR of the "Clear" switch and of the internal error when the INAR switch is not inserted.
- CI891=1 (025-2) this command is issued, during the E2/E3 status of phase α , when an HLT instruction is performed or if the "Step-by-step" switch is inserted and enabled.
- ALS71=1 (025-1) this signal is issued after a work cycle of the C.P.U. (RETOG=0) in the following cases:
 - the PAPA switch is inserted (AMICB=0)
 - the rotary switch is neither in normal position, nor in position 8 for recording in memory (ALSOA=0)
- ALS5A (025-7) this signal is generated during the E6 status in the phase α of the jump instructions (CI38) when:
 - the ACOV or ACON switches are inserted;
 - the related condition be verified.

6.5. Starting and recycling of the main timing

The main timing is obtained through 4 Delay Line boards (LIRI) with a delay of about 600 ns each. Every LIRI is driven from a CEMA circuit (pulses generator) which generates a negative pulse with a period equal to about 160 ns.

The pulses which pass through the LIRI are taken and powered with tapping circuits (CISP) which supply positive pulses of 100 ns $\pm 10\%$.

The name of the pulses is of the Txxx type where xxx varies from 000 to 110 (refer to figure 5 on the following page).

The starting of the timing is obtained by means of the trailing edge of the ALDEA signal (022-15).

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After the powering-on of the machine the timing starts pressing the "Clear" switch.
 In fact, the pressure of "Clear" (signal ASGA) causes the setting of the FF ACI21 (022-9) and AST21 (022-23).
 When the "Clear" switch is released, the FF ACCIC1 (022-14) and AST01 (022-20) are set.
 ALDEA then passes to 0 and starts the timing that from this moment onward cycles automatically through the cyclic reset and set of the ACIC FF.
 The ACIC1 FF is reset by the TO10 pulse and it is set by the TO901 with the condition PODIB = "1".
 PODI is the FF which stores the LOLL diagnostic instruction performance causing an increase of the cycle of about 130 ns.
 In fact, if PODIB is at "0" the recycling occurs with the pulse TIO5 instead of the TO90.

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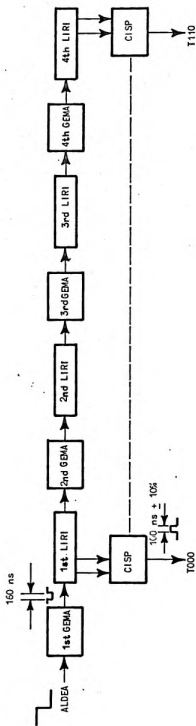


Fig. 5 - Main delay line

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The possible reasons for a stop of the timing act resetting the FF ASTO.

Here they are:

- a) ATEMB = 0 (022-17) insertion of the PATE switch;
- b) AST61 = 0 (022-16) is checked when there is an Internal Error (GEST1) after a memory reading (CO301) with a valid address (MEVA1) and with the INAR switch not inserted (AINAF);
- c) AST71 = 0 (022-22) is checked when an invalid memory position (INVAB = 0) is addressed with the INAR switch not inserted (AINAF = 1).

The timing can be restarted through the "Start" switch or the "Clear" switch which act setting the FF ASTO through the signals AVIA and ASGA (022-26).

6.6. Sequence logic matrix (MLS)

6.6.1. General

The MLS is the device which establishes which operations must be performed by the processor for every work cycle. It consists of a logic network which supplies the commands required to activate the various parts of the internal logic.

The MLS is on its turn driven and conditioned by the following devices:

- a) FO register, which identifies the type of instruction under way;
- b) SA register, which supplies the configuration of the status to be performed;
- c) FA00-06 register which stores special variable conditions;
- d) RO register which supplies special decodings;
- e) FF URPE which stores the carry-overs of the arithmetic unit operations;
- f) various other machine signals which are not listed here as their importance is irrelevant (refer to IBD 140130690 fig. 8).

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The commands act generally when they have a logic level "1".

The commands are thus divided:

- COxx and CIxx are the commands which interest the performance of the internal instructions. These commands are generally timed in the suitable way, because of the fact that some operations may be performed twice within the same cycle (e.g. the operations of the counting network). The commands required to perform the operations of the first part of the cycle are called of the 1st phase (normally they are the COxx commands). The commands performing the same operation in the second part of the cycle are called of the 2nd phase (normally they are the CIxx commands);
- CAxx are the commands after the timing, i.e. the "phased commands";
- CExx are the commands related to the check of the data transfer with the peripheral units;
- CUxx are the commands establishing the configuration of the future status which must be stored in the SO or SI registers.

6.6.2. MLS performance

As the MLS consists of a combinatory logic whose detailed description at the individual signals level would be of no practical use, refer to the descriptions of the "Flow charts" No. 14023130 and the "Timing charts" No. 140241370. Here below there is a general explanation of the names of the signals composing the matrix.

- DOxx: decodings of the FO function register;
- DIxx: decodings of the SA status register;
- DUxx, DCxx: decodings of various conditions;
- DIxx in AND with DOxx give origin to:
 - DExx or DAxx which in turn in AND with DUxx or DCxx form:
 - ECxx, EDxx, ECxx which are the "calls" for the commands; should these calls be common to several

CONF. A 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100	UNIT	REV. 30004122 o/a
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commands, they will assume instead the following names:

- CMxx if related to future status commands;
- CBxx if related to 1st phase commands;
- CDxx if related to 2nd phase commands.

6.6.3. List of signals issued by the MLS

In the list below the commands are grouped by logic function and in alphanumeric order.

6.6.3.1. Commands to load the registers

OPERATION	1st PHASE	2nd PHASE	COMMENTS
NI → P0	C000	CI00	
NI → V1	01	01	
NI → V2	02	02	
NI → V3	03	03	
NI → V4	04	04	
NI → L1	---	05	
NI ₂₁ → L2	06	06	
NI → L3	---	07	
NI ₂₁ → P0	---	08	
NI ₄₃ → RI	---	09	

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6.6.3.2. NO knot selection command

OPERATION	1st PHASE	2nd PHASE	COMMENTS
P0 → NO	C010	CI10	
V1 → NO	11	11	
V2 → NO	12	12	
V3 → NO	13	---	
V4 → NO	14	---	
L1 → NO	---	15	
L2 → NO ₂₁	16	16	
L3 → NO	---	17	
FORC. → NO ₂₁	18	---	
FORC. → NO ₄₃	---	19	
A.M. → NO	---	20	
RI → NO ₄₃	---	21	

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6.6.3.3. VO, BO, RO loading commands

OPERATION	1st PHASE	2nd PHASE	COMMENTS
READING	C030	- - - -	This command, beside starting the reading operation and the memory regeneration, enables the setting of the Flip-Flop of INTERNAL ERROR and the RO loading. This command prevails on the other RO loading commands
WRITING	C031	- - - -	
NO \rightarrow RO ₄₃	- - - -	CI32	The simultaneous absence of these 3 commands and of C030 determines the clearing of RO
NO \rightarrow RO ₂₁	- - - -	33	
NE \rightarrow RO	- - - -	34	
Reset Int. Error	C035	- - - -	
Enable set of AVER, ALTO	- - - -	CI38	It is called in the E6 E7 status of phase α by the status decoder.
Reset AVER	- - - -	CI39	It resets the FF AINI & PUC1 too

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6.6.3.4. Count and Arithmetical Unit commands

OPERATION	1st PHASE	2nd PHASE	COMMENTS
COUNT MINUS	C040	CI40	Should the COUNT MINUS not be present, there is COUNT PLUS
COUNT 00	41	41	Should both these commands be absent, B0 is transferred.
COUNT 04	----	42	
BLOCK 03	----	43	
BLOCK 07	----	44	
LOGICS	----	45	
DEC. - AND	----	46	<p>The content of URPU passes in URPE at the beginning of every status, always when there are not the set and reset commands. The reset command is prevailing on the set commands. URPU is loaded with the carry over of the arithmetical unit (UA) every time there is a command of unloading of UA → NI if it is a C.P.U. cycle. This command prevails on the set and reset.</p> <p>It does not process the most significant part.</p> <p>It does not process the less significant part.</p>
SUPT. - ORE	----	47	
Set URPE and URPU	C048	----	
Reset URPE and URPU	C049	----	
UA ₁ → URPU	----	50	
URPE → UA ₂	----	51	

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6.6.3.5. NI knot selection commands

OPERATION	1st PHASE	2nd PHASE	COMMENTS
RO ₂ → NI ₄	----	CI60	In the first phase the counting network output is always selected; in the second phase it is selected again only if there are not the commands corresponding to UA → NI and RO → NI. This last one prevails on all of them.
RO ₂ → NI ₃	----	61	
RO ₂ → NI ₂	----	62	
RO ₂ → NI ₁	----	63	
RO ₁ → NI ₄	----	64	
RO ₁ → NI ₃	----	65	
RO ₁ → NI ₂	----	66	
RO ₁ → NI ₁	----	67	
U.A. → NI ₄₃	----	68	It commands also BO ₄₃ → U.A.
U.A. → NI ₂₁	----	69	It commands also BO ₂₁ → U.A.

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6.6.3.6. Commands to set and reset FF of condition

OPERATION	1st PHASE	2nd PHASE	COMMENTS
Set FIO0	---	CI70	Reset prevails on set
Set FIO1	---	71	
Set FIO2	---	72	FIO2 is used only by external sequences
Set FIO3	---	73	
Set FIO4 = RIPO	---	74	
Set FIO5 = DIVE	---	75	
Set FIO6 = MASC	---	76	
Set ADIR	---	77	
Reset ADIR	---	78	
Reset FIO0	---	80	
Reset FIO1	---	81	
Reset FIO2	---	82	
Reset FIO3	---	83	
Reset FIO4 = RIPO	---	84	
Reset FIO5 = DIVE	---	85	
Reset FIO6 = MASC	---	86	
Set ALAM	---	87	
Reset ALAM	---	88	
Set ALTO	---	89	

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6.6.3.7. Commands to force in NO knot

OPERATION	1st PHASE	2nd PHASE	COMMENTS
"1" → N000 (N008)	C090	---	The commands of a single forcing act on the 1st and 2nd phase depending on the presence of C018 or CI19.
"1" → N001 (N009)	91	---	
"1" → N002 (N010)	92	---	
"1" → N003 (N011)	93	---	
"1" → N004 (N012)	94	---	C018 in the 1st phase forces in N000 - 07
"1" → N005 (N013)	95	---	CI19 in the 2nd phase forces in N008 - 15
"1" → N006 (N014)	96	---	
"1" → N007 (N015)	97	---	

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OPERATION	1st PHASE	2nd PHASE	COMMENTS
RO → RA	CE00	---	
RO → RE	01	---	
Enable channel selection	02	---	Admits AEBE
Reset I/O	03	---	Resets the errors
Enable the set of external error	05	---	
Enable the set of error 1	06	---	
Set I/O for CAN1, CAN2, CAN3	07	---	
Set VICU	08	---	
Issue TU101	09	---	
Issue TU201	10	---	
Issue TU301	11	---	
Issue TU103	12	---	
Issue TU203	13	---	
Issue TU303	14	---	
Issue FIRU	15	---	
Loads buffer	16	---	for CAN2
End of print	17	---	
Enable reset RIAP	18	---	It enables the reset of FF for the cycle attribution requests
Reset select ion CAN3	19	---	

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6.6.3.9. Future states commands

OPERATION	1st PHASE	2nd PHASE	COMMENTS
Set S000	---	CU00	The reset prevails on the set
Set S001	---	01	The reset prevails on the set
Set S002	---	02	The reset prevails on the set
Set S003	---	03	The reset prevails on the set
Set S004	---	04	The reset prevails on the set
Set S005	---	05	The reset prevails on the set
Set S006	---	06	The reset prevails on the set
Set S007	---	07	The reset prevails on the set
Reset S000	---	10	The reset prevails on the set
Reset S001	---	11	The reset prevails on the set
Reset S002	---	12	The reset prevails on the set
Reset S003	---	13	The reset prevails on the set
Reset S004	---	14	The reset prevails on the set
Reset S005	---	15	The reset prevails on the set
Reset S006	---	16	The reset prevails on the set
Reset S007	---	17	The reset prevails on the set
Forces Future Stat. S0;S1	---	CU20	The reset prevails on the set

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6.7. Cycle attribution logic6.7.1. General

As it has already been mentioned, the MLS is the device which determines, for every cycle of the Delay Line, the operations which must be performed by the computer. Neglecting the special cases, and the ones due to the use of the maintenance panel, these operations may be:

- operations concerning the performance of external instructions, or the start of external instructions;
- operations concerning the data exchange between computer and peripheral units.

Considering that:

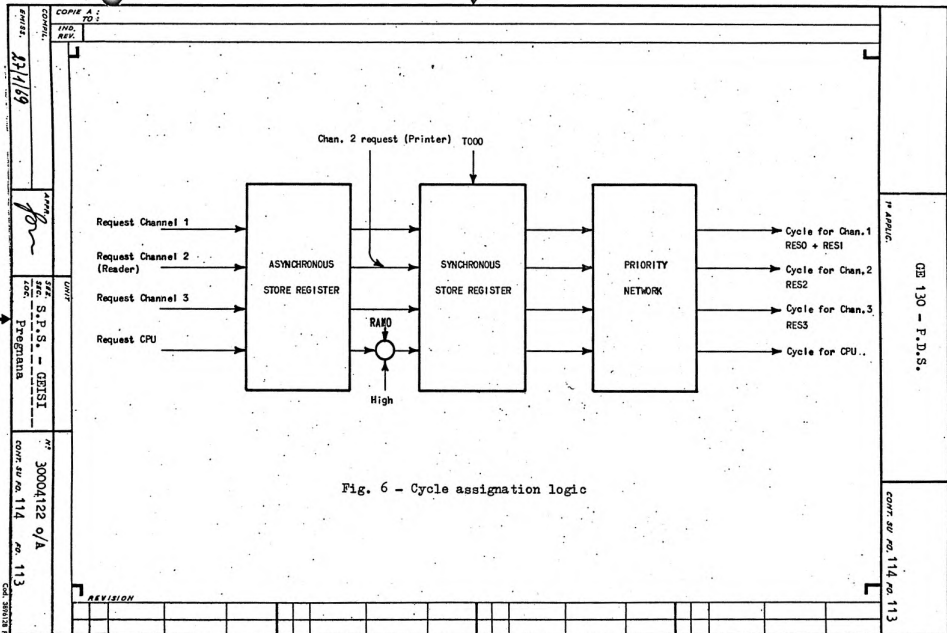
- the internal instructions can work in an overlapped mode with the external operations;
- the external instructions concerning different channels can be performed in overlapped mode;
- the use of a different operations sequence corresponds to every work channel;
- the priority of the various work channels is the following:

1st channel	1 for external operations
2nd channel	3 for external operations
3rd channel	2 for external operations
4th channel	1 for internal calculation;

it is evident that there is the necessity to establish, at the beginning of every cycle to which the work channel must be attributed, the cycle itself.

The cycle attribution is established through a circuit which can be summarized as per fig. 6 in the next page.

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6.7.2.

Description of the asynchronous storage circuit

The asynchronous storage circuit consists of the following FF:

- RCOO (130-2) cycle request for CPU.
It is reset with the CE18 (enable RIAP reset) command while a cycle is performed for the CPU (RIUC=1).
The CPU is thus waiting for the external triggers of command received.
RCOO is set by the clear signal (CAGUF=0) with the signal of command received by the peripheral unit (RBII=1), with the insetion of the SITE key which frees the waitings (RAITI=1) and finally with the dissection of the channel 1 (PUC16=0);
- RCO1 (129-4) cycle request for channel 1
It is set with the OR of the cycle request triggers relative to channel 1 (RAIO1, 129-1) if the instruction under way (RIVEF=1) is not over.
It is set also when the SITE key is inserted (RAITI=1) during a transfer of channel 1 (RASI2=1 129-6).
It is reset during the performance of a cycle of channel 1 (RES16=1) if the command Enable Reset RIAP (CE18) is issued or at the end of the transfer on channel 1 (RASI2=0);
- RCO2 (129-11) Cycle request from reader for channel 2
It is set with the trigger LU08 arriving from integrated reader or when the SITE key (RAITI=1) is inserted during the transfers of the reader with channel 2 (PC221=1, 119-14).

Note: the requests from printer do not act on RCO2 but are set in OR with RCO2 (RIMZA).

RCO2 is reset during the performance of a cycle on channel 2 (RES26=1) if the command CE18 is issued or at the end of the transfer (PC221=0);
- RCO3 (129-18) cycle request for channel 3
It is set with the OR of the cycle request triggers relative to channel 3 (RA301=1, 129-15) if the instruction under way (RIVAF=1) is not over and if the additional performances of the GE 130 are enabled (FUL4F=1).

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It is reset also when the SITE key (RAITI=1) is inserted during a data transfer on channel 3 (PUC36=1). RCO3 is reset during the performance of a cycle on channel 3 (RES36=1) if the CE18 is issued, or at the end of the transfer (PIC32=0).

By pressing "Clear" the FF RCO1, RCO2, RCO3 are reset and the FF RCO0 is set.

6.7.3. Description of the synchronous storage circuit

After the requests of the various channels have been stored in the related FF in an asynchronous mode, they are transferred with the pulse T000 (which is the first one of the Delay Line) in the synchronous storage circuit consisting of the FF RIA0 (131-3), RES1 (131-12), RIA2 (131-19), RIA3 (131-22).

RCO1 is transferred directly in RES1.

RCO3 is transferred directly in RIA3.

RCO2, set in OR with the requests from MZ (RCA21, 129-12), is transferred in RIA2.

RCO0 is conditioned by the signals ALTOF and RAMO2.

When the FF ALTOF is reset, the cycle requests from CPU are not served and therefore the internal calculation is stopped.

This counter consists of the FF RAMO (133-13) and RAM1 (133-14) and counts with the pulse T010.

6.7.4. Priority network

The priority network (131) generates the cycle attributions in function of the requests of the synchronous storage circuit observing the following priority:

- the requests concerning channel 1 (RES1, 131-7) are certainly fulfilled as they have the highest priority;
- the requests of channel 3 (RIA3) having an average priority are fulfilled only if there are no requests of channel 1 (RES36, 131-17, = RIA3 . RES1);

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- the requests of channel 2 (RIA2) are fulfilled only if there are no requests of channel 1 and 3.
RES26 (131-14) = RIA3 . RES1 . RIA2;
- the requests of CPU (RIA0) are fulfilled only if all the other requests are not present.
RIUC (131-5) = RIA0 . RES1 . RIA3 . RIA2.

Note: the signal RES0 is issued when the cycle has been attributed to the CPU or to channel 1.

When all the cycle requests are not present, the MLS performs the states with configuration 0/0. These states, called of display, do not perform any significant operation.

6.7.5.

Logic of variation of the cycle period

Depending on the logic level of the signals FULO (133-11) and FULI (133-9) arriving from strappings assembled during installation, the FF RAMO will be always at "1" (cycle period of the CPU = 2 μ s) or at "1" for the period of 2 μ s with a period of 4 μ s (cycle period of the CPU = 4 μ s), or at "1" for a period of 2 μ s with a period of 6 μ s (cycle period of the CPU = 6 μ s).

The correspondence between the configuration of the signals FULO and FULI and the cycle period is the following:

FULO	FULI	Cycle period
I	I	6 μ s
0	I	4 μ s
0	0	2 μ s

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6.8. Logic to drive the MLS6.8.1. General

The operations that the CPU must perform are controlled by the MLS, which in its turn is driven by special machine devices called sequencers.

The sequencers allow the performance status by status of the operations that the program has attributed them. The orderly sequence of the simultaneous operations (up to three allowed) is obtained through the logic for the cycle attribution, whose signals select from time to time the interested sequencer.

6.8.2. Performance logic

The internal calculation and the data transfer on channel 1 cannot be overlapped.

Both these operations use the sequencer S0. In particular, during the data transfer phase on channel 1, the status in which the character is exchanged between CPU and the peripheral unit has on the SA register the hexadecimal value B9 (in the case of data input with packing on channel 1 two subsequent states B9 and B1 are requested). In the interval between one status of character exchange and the following one, the CPU performs the not operative states (B8), calling again in SA, through the signal RES0, for the configuration present in the sequencer S0, which has the hexadecimal value B8.

The character exchange cycle on channel 1 is characterized by the simultaneous presence of the signals RES0 and RES1.

The signal RES0 calls in SA for the content of S0 (B8) while the signal RES1 forces in SA00 the logic value "1". The content of SA therefore in this cycle has the hexadecimal value B9, which is the status in which the real character exchange between CPU and peripheral unit is possible.

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- The performance phase of a data transfer with the channel 2 is made possible through a special sequencer sustained by the SI register. The SI register consists of 4 bits and it is loaded, at the end of a cycle assigned to channel 2, with the next status required in order to go on with the operation which is under way.
The unloading of SI in SA occurs when the machine cycle has been attributed to channel 2, i.e. with the presence of the RES2 signal.
- If the cycle has been attributed to channel 3 the use of a real sequencer is not necessary.
In fact the status related with the data exchange through channel 3, both in input and in output, has the configuration 0/1.
It is therefore enough to force "1" in the bit 00 of the register SA which drives the MLS, through the RES3 signal.
- If there are not the requests relative to the data exchange channel and the channel 1 has not been started, the signal RES0 causes the transfer of S0 in the register driving the MLS. In this case, S0 contains the configuration related to any status of phase α or β of the internal instructions or of the general phase β of the external instructions.

6.9. Registers and knots6.9.1. P0 register

It is the program addresser register, i.e. the register used to scan the positions of the memory in which the program instructions are recorded.

It is a register with 16 bits which can be loaded with the content of the NI knot through the commands C000 or C100 in 1st or 2nd phase.

The outputs of the P0 register drive the NO knot when when the commands C010 or C110 are issued in the 1st or 2nd phase.

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6.9.2. V1 register

It is a register with 16 bits which is used as the addresser of the field which contains the 1st operand. It is loaded during the 1st or 2nd phase by the NI knot through the commands C001 or C101. It drives the NO knot in the 1st or 2nd phase through the C011 or C111.

6.9.3. V2 register

It is a register with 16 bits which is used as the addresser of the field containing the 2nd operand. In some cases it is used as the addresser of the 1st operand if the instruction has only one address (e.g.: the sub-field of the external instructions). It is loaded by the NI knot in the 1st or 2nd phase through the commands C012 or C112.

6.9.4. V3 register

It is a register with 16 bits. It is used as an addresser during the performance of the external instructions using channel 3. It is loaded from the NI knot in the 1st or 2nd phase respectively through the commands C003 and C103. It drives the NO knot in the 1st phase through the command C013. It is loaded initially from the 5th and 6th character of the sub-field of the external instructions.

6.9.5. V4 register

It is a register of 16 bits which is used as an addresser during the performance of the external instructions using channel 2. It is loaded by the NI knot in the 1st or 2nd phase through the commands C004 and C104. It drives the NO knot in the 1st phase through the command C014.

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6.9.6. RI register

It is a register with 8 bits.

It is used to store the photodisc codes arriving from the integrated printer. Also the characters arriving from the integrated reader pass through this register but they are not used.

It is loaded with the bits 08 - 15 of the NI knot during the 2nd phase through the command CIO9.

It drives the most significant bits of the NO knot only during the 2nd phase through the command CI21.

6.9.7. L1 register

It is a register with 16 bits, it is used to store the length of the operands or for information in transit. It is loaded by the NI knot during the 2nd phase through the command CIO5.

It drives the NO knot during the 2nd phase through the command CI15.

6.9.8. L2 register

It is a register with 8 bits used as auxiliary register. It is loaded with the less significant part of the NI knot during the 1st or 2nd phase through the commands CO06 and CIO6.

It drives the less significant part of the NO knot during the 1st or 2nd phase through the command CO16 and CI16.

6.9.9. L3 register

It is a register which expresses the length of the operands related with the instructions operating on channel 3.

It is loaded initially by the 3rd and 4th character of the sub-field of the external instructions.

It is loaded by the NI knot during the 2nd phase through the command CIO7.

It drives the NO knot during the 2nd phase through the command CI17.

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6.9.10. Definition of "knot"

By knot we mean an AND-OR logic network of data transit which does not store. Several information from registers or commands suitably combined converge in this network, through suitable enable commands.

6.9.11. NO knot

The NO knot may be driven by the following registers:

P0, V1, V2, V4, L1, L2, RI, V3 and L3.

The L2 register (8 bits) drives always the 8 less significant bits of NO.

The RI register (8 bits) drives always the 8 most significant bits of NO.

In addition, the NO contains:

- the forcings from program
- the signals of forcing arriving from the maintenance panel (AM keys).

The forcings from program consist of 8 commands (C090 - C097) which can force the first or the second 8 bits of NO.

The other two commands C018 and C119 enable the real forcing and establish in what part of the knot to perform it. (refer to fig. 7).

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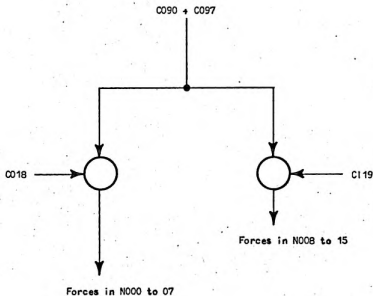


Fig. 7 - Present example

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The forcings from maintenance panel are enabled all together (16 bits) from CI20.

The NO knot may transfer its content in:

VO - memory addresser

This transfer occurs always at the beginning of the cycle, and determines the memory address selected during the status.

BO - In the 1st phase this transfer occurs without any condition.

In the 2nd phase this transfer occurs only if the transfer commands from NO in RO are not present. If instead there is a transfer of NO in RO the content of BO remains ~~the one~~ which was loaded in the 1st phase.

RO - it may be loaded with the first 8 bits

6.9.12. RO register

It is a register with 8+1 bit.

It is cleared without conditions with the pulse TO20.

It may be loaded by:

- the read signal arriving from memory;
- the outputs of the NE knot in which the data from the peripheral units converge;
- the bits 00 - 08 of the NO knot which are transferred in the bits R000 - R008;
- the bits 08 - 15 of the NO knot which are transferred in the bits R000 - R007.

The transfer command of MEM in RO (C030) has the precedence on the other loading commands.

The RO register may drive with its outputs:

- The arithmetical unit.
- Only the bits 00 - 07 are considered.

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- The NI knot.
Only the bits 00 - 07 which may be transferred in each one of the 4 parts of the NI knot.
- The register RA and RE
- The network to examine the condition of the peripheral units
- The network of check
- The memory inhibition circuits.

6.9.13. VO register

It is a register with 16 bits which is loaded without conditions during the 1st phase with the T020 from the content of the knot.

It is used to address the memory circuits and therefore to establish in which position the data should be read and written.

It supplies with its outputs the decodings:

(Ch 068-3) VOZ06 = 1 configuration 0 in the less significant part (V002 - V000).

(Ch 068-3) VOZ16 = 1 configuration 2 in the less significant part (V007 - V000).

(Ch 068-14) VOZ26 = 1 configuration 81 in the less significant part (V007 - V000).

(Ch 068-20) VOZ36 = 1 configuration 161 in the less significant part (V007 - V000).

(Ch 287-07) VOZ41 = 1 configuration 164 in the less significant part (V007 - V000).

If these data are to be visualized, it is therefore enough to unload in the NOKnot the register that is to be visualized. If some forcings are to be done, the required configuration is unloaded in the NO knot through the AM keys of the maintenance panel.

This configuration is transferred in B0. From B0, through the count network (which will perform no variations, as there are not commands related to them), the configuration is transferred in the NI knot.

From the NI knot the configuration can be stored in the required register, through the related transfer command.

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6.9.14. BO register

It is a register with 16 bits.

During the 1st phase, it is loaded without conditions by the NO knot.

During the 2nd phase, it is loaded by the NO knot only if the commands of transfer from NO in RO are not present. If these are present, the content of BO is the one which was loaded during the 1st phase. With its output, it drives without conditions the counting network or it may drive the arithmetical unit (UA) through the bits 00 - 07 or through the bits 08 - 15.

The corresponding commands (CI68 and CI69) determine in which half of the NI knot the result of the UA operation must be unloaded.

BO is the register used to visualize the various registers on the operating panel through the use of the maintenance panel just because of its characteristics:

- of being loaded always during the 1st phase by the content of NO;
- of driving without conditions the counting network.

6.9.15. NI knot

It may be driven by:

- the outputs of the counting network. This occurs always during the 1st phase. During the 2nd phase the driving occurs only if the corresponding commands of RO in NI and of UA in NI are not present;
- the 1st or 2nd part of RO which may be transferred in anyone of the 4 parts of NI (CI60 - CI67) during the 2nd phase;
- the UA output always during the 2nd phase. The UA may drive the 8 most significant (CI68) or the 8 less significant (CI69) bits. The same commands determine also which part of BO must drive the UA to perform the operation.

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The quartets of UA may drive the NI knot only if the corresponding RO commands in NI are not present. These in fact have the highest priority. The priority of the various load operations is obtained acting on the signals generation (Ch. 100 - 103):

- NIRxx concern the loading from RO and are conditioned only by their related commands;
- NIUxx concern the loading from UA and are conditioned, beside from the UA command in NI also by the absence of the related NIRxx;
- NIRxx concern the loading from the counting network and are generated when the corresponding NIRxx and NIUxx are absent.

6.9.16. FO register

It is a register with 8 bits.

It stores the function code of the instructions under way.

It is loaded through the NI knot during the status E2/E3 of phase α with the command C108. It goes to to drive the MLS.

6.9.17. S0 register

The S0 register is the main sequencer of the processor. It is used to establish the sequence:

- of phase α of all the internal and external instructions;
- of phase β of the internal instructions;
- of the organization phase (general β) of the external instructions;
- of the phase β of transmission and reception of data related to channel 1;
- of program loading.

It drives the NA knot when the cycle has been attributed to CPU or channel 1.

It is loaded by the outputs of the logic network of the future status (SU00 - SU07) when the signal SOC01 (116 - 15) is activated.

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SOC01 may be activated only if the RICI key is not inserted (ARICA=1).

It is activated in the following cases:

- the FF ARES has been set through "Clear". In this case, when the machine performs the first status 0/0, the set of SO07 (CU07) is sent. As also the strobe of SO starts the configuration 8/0 is forced in SO;
- the rotary switch is in position of forcing in SO (AF436=1).
When a cycle is attributed to the CPU pressing the "Start" (RET06=1) the keys AM00 - 07 are forced in SO;
- the rotary switch is in normal position (AF326=1) and the cycle performed was for the CPU or channel 1 (RET06=1).
In this case, the configuration concerning the future status is stored in SO.

6.9.18.

SI register

The SI register of 4 bits is the sequencer used for the data exchange with the peripheral units through channel 2. It contains always the "C" configuration (1100) when there is a data input (integrated reader). It contains different configurations when work is done with an integrated parallel printer (refer to the external sequence of channel 2). It drives the NA knot when the cycle has been attributed to channel 2. It is loaded with the first 4 bits of the logic network of future status through the signal SIMA1=1 in the following cases:

- after the execution of a cycle of channel 2 (RET26=1, Ch 108 - 1)
- when the command CU20 to force the status in SI is issued. (BAS1=1, Ch 218-5).
This occurs during the "DC" status of general β phase in order to force the configuration "C" in SI.

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6.9.19. NA knot

This knot may be driven:

- by the 8 bit S0 register.

This occurs when the work cycle has been attributed to the CPU or to channel 1 (RES06=1 Ch 109-4) if the rotary switch is in the central position (AF326=1 Ch 109-1);

- by the SI register which drives the 4 less significant bits.

This occurs when the cycle has been attributed to channel 2 (RES26=1 Ch 109-2).

The four most significant bits stay to zero as they are not driven.

In addition action can be taken on the individual bits in the following way:

- NAO0 (109-12) is forced to 1 when the work cycle is attributed to channel 1 (RES16=1) or to channel 3 (RES30=1);
- NAO3 (109-3) is forced to 1 when the work cycle has been attributed to the CPU (RES06=1) and the rotary switch is not in the central position (AF32C=1).

The content of the NA knot is stored with the T010 pulse in the SA register which drives directly the MLS.

6.9.20. SA register

It is the register which drives directly the MLS circuits. It is loaded by the NA knot at every pulse T010.

Beside the MLS, it drives also the logic network which generates the future status configuration.

6.9.21. FI and FA registers

They are the registers containing special conditions which occur during the performance of an instruction. They are 7 FF (F100 - F106) on which the sequence acts through the set and reset commands timed by the T106 pulse which is one of the last pulses of the Delay Line.

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At the beginning of the following cycle, the configuration of the FF F100 - F106 is unloaded in the FF FA00 - FA06 through the pulse T010 (112-4). The FA register is the one used to condition the MLS. When possible, the same meaning has been attributed to every condition FF.

FA03 stores always the condition of end of length of the second operand.

FA04 and FA05 store the qualitative result (respectively RIPO and DIVE of the 115/1 and 115/2) and in some cases they are used also as condition FF.

FA06 is the FF which conditions the interruption requests. It is never used as a condition FF.

The set commands of the register FI are the commands CI70 - CI76.

The reset commands are the commands CI80 - CI86.

If the commands of set and reset are issued simultaneously from a sequence, the reset command prevails on the set.

This is obtained through the signals FIS0A - FIS6A (112-5) which may go to "0", and therefore set the FF FIxx, only if the corresponding reset commands (CI80 - CI86) are not present.

The signals FIA0 - FIA6 (112-10) serve, in every cycle, to copy the previous FA configuration in FI, should both the set and reset commands be absent.

6.10. Loading logic of the future status

The logic network of future status generates the configuration of the next status to be performed, which must be stored in S0 or SI register.

It has as an output the signals SU00 - SU07.

It uses as inputs the configuration of the present status (provided by the SA register) and the commands of future status CUxx generated in the present status by the MLS.

The CUxx commands are variable in function of the present status and of the machine conditions.

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6.10.1. FF RETO and RET2

The function of these two FF is the one to store to which work channel the present cycle has been attributed in order to allow to unload the configuration of future status in the related sequencer (SO or SI).

For this reason the cycle attribution signals (RESO or RES2) cannot be used, as the future status loading occurs with the TI06 pulse.

The TI06 pulse is a pulse following the T090 pulse of normal recycle, so that the loading of the future status is overlapped with the phase of the following cycle priority.

It is therefore evident that the signals RESO or RES2 could lack in function of the new cycle attribution. Therefore the signal RESO is stored in the FF RETO and the signal RES2 in the FF RET2 with the pulse T010.

6.11. Counting network

The counting network performs operation of count +1 or -1.

The counting network may perform two operations during the same status.

It is driven by the B0 register.

The outputs of the counting network (BU00 - BU15) drive the NI knot.

The counting network is conditioned by the following commands:

- C040 - CI40 Command to count -1.
During an operation of the counting network, the count +1 is enabled if this command is absent.
- C041 - CI41 Command to count bit 00
The counting operation is performed starting with bit B000 onward.
- CI42 Command to count bit 04
The counting operation is performed starting with bit 04 onward leaving bits 00- 03 unchanged.
- CI43 Command to block bit 03
The carryover due to the 4th bit (bit 03) is not unloded in the 5th bit (bit 04).

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- CI44 Command to block bit 07

The carryover due to the 8th bit (bit 07) is not unloaded in the 9th bit (bit 08).

In the following table there are all the possible operations performed by the counting network in function of the commands related to it even if some of them are not used by the sequences.

COUNTS COUNTS COUNTS BLOCKS BLOCKS MINUS BIT 00 BIT 04 BIT 03 BIT 07					OPERATIONS PERFORMED BY THE COUNTING NETWORK
CO40 CI40	CO41 CI41	CI42	CI43	CI44	
0	0	0	0	0	Transfer of bits 00 - 15
0	0	0	0	1	Transfer of bits 00 - 15
0	0	0	1	0	Transfer of bits 00 - 15
0	0	0	1	1	Transfer of bits 00 - 15
0	0	1	0	0	Counts +1 on bits 04 - 15
0	0	1	0	1	Counts +1 on bits 04 - 07 and transfers the others
0	0	1	1	0	Counts +1 on bits 04 - 15
0	0	1	1	1	Counts +1 on bits 04 - 07 and transfers the others
0	1	0	0	0	Counts +1 on bits 00 - 15
0	1	0	0	1	Counts +1 on bits 00 - 17 and transfers the others
0	1	0	1	0	Counts +1 on bits 00 - 03 and transfers the others
0	1	0	1	1	Counts +1 on bits 00 - 03 and transfers the others
0	1	1	0	0	Counts +1 on bits 00 - 03 and on bits 04 - 15
0	1	1	0	1	Counts +1 on bits 00 - 03 and on bits 04 - 15 and transfers the others
0	1	1	1	0	Counts +1 on bits 00 - 03 and on 04 - 15
0	1	1	1	1	Counts +1 on bits 00 - 03 and 04 - 07 and transfers the others

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COUNTS COUNTS COUNTS BLOCKS BLOCKS
MINUS BIT 00 BIT 04 BIT 03 BIT 07

OPERATIONS PERFORMED

BY THE COUNTING NETWORK

CO40 CO41

CI40 CI41 CI42 CI43 CI44

1	0	0	0	0
1	0	0	0	1
1	0	0	1	0
1	0	0	1	1
1	0	1	0	0
1	0	1	0	1
1	0	1	1	0
1	0	1	1	1
1	1	0	0	0
1	1	0	0	1
1	1	0	1	0
1	1	0	1	1
1	1	1	0	0
1	1	1	0	1
1	1	1	1	0
1	1	1	1	1

Transfer of bits 00 - 15
Transfer of bits 00 - 15
Transfer of bits 00 - 15
Transfer of bits 00 - 15
Counts -1 on bits 04 - 15
Counts -1 on bits 04 - 15 and
transfers the others
Counts -1 on bits 04 - 15
Counts -1 on bits 04 - 15 and
transfers the others
Counts -1 on bits 00 - 15
Counts -1 on bits 00 - 07 and
transfers the others
Counts -1 on bits 00 - 03 and
transfers the others
Counts -1 on bits 00 - 03 and
transfers the others
Counts -1 on bits 00 - 03 and
on 04 - 15
Counts -1 on bits 00 - 03 and 04 - 07
and transfers the others
Counts -1 on bits 00 - 03 and 04 - 15
Counts -1 on bits 00 - 03 and 04 - 07
and transfers the others

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6.12. - Arithmetic unit

6.12.1. - General principle

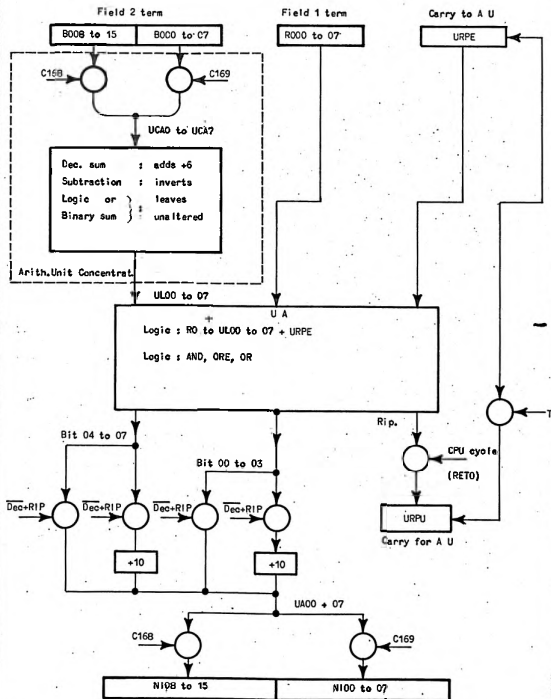


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6.12.2. General

The arithmetical unit can perform logic type operations (OR, AND, Exclusive OR), or of arithmetical, binary or decimal type.

The arithmetical unit is driven through 5 commands issued by the MLS.

The table on the following page gives all the operations performed by the arithmetical unit in function of the configurations of such commands.

The operand 1 of the operation to be performed is stored in R0, and is transferred unchanged to the arithmetical unit.

The operand 2 is taken from the B0 register.

Two commands determine whether the most or the less significant part of the B0 register must be used.

The command CI68 determines the use of B0⁴³ (08 - 15).

The command CI69 determines the use of B0²¹ (00 - 07).

In the table B0 is considered as a register with 8 bits only.

Note: It must be noted that some operations listed on the table of the following page are not used by the sequences.

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DECIM. SUBTR. URPE UA ₁ LOGIC AND ORE IN IN OR OR UA ₂ URPU					OPERATIONS PERFORMED BY THE ARITHMETICAL UNIT	
CI45	CI46	CI47	CI51	CI50		
0	0	0	0	0	Binary addition	RO ₂₁ + BO ₂₁
0	0	0	0	1	Binary addition	RO ₁ + BO ₁
0	0	0	1	0	Binary addition	RO ₂ + BO ₂
0	0	0	1	1	Binary addition	URPE in URPO invalid result
0	0	1	0	0	Binary subtraction	RO ₂₁ - BO ₂₁
0	0	1	0	1	Binary subtraction	RO ₁ - BO ₁
0	0	1	1	0	Binary subtraction	RO ₂ - BO ₂
0	0	1	1	1	Binary subtraction	URPE in URPU invalid result
0	1	0	0	0	Decimal addition	RO ₂₁ + BO ₂₁
0	1	0	0	1	Decimal addition	RO ₁ + BO ₁
0	1	0	1	0	Decimal addition	RO ₂ + BO ₂
0	1	0	1	1	Decimal addition	URPE in URPU invalid result
0	1	1	0	0	Decimal subtraction	RO ₂₁ - BO ₂₁
0	1	1	0	1	Decimal subtraction	RO ₁ - BO ₁
0	1	1	1	1	Decimal subtraction	RO ₂ - BO ₂
0	1	1	1	1	Decimal subtraction	URPE in URPU invalid result
1	0	0	0	0	Clearing of UA	UAXX = 0 (XX = 00 - 07)
1	0	0	0	1		
1	0	0	1	0		
1	0	0	1	1		

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CONT. SU PD. 137 PD. 136

DECIM. SUBTR. URPE UA ₁ LOGIC AND ORE IN IN OR OR UA ₂ URPU					OPERATIONS PERFORMED BY THE ARITHMETICAL UNIT
CI45	CI46	CI47	CI51	CI50	
1	0	1	0	0	Exclusive OR
1	0	1	0	1	Exclusive OR
1	0	1	1	0	Exclusive OR
1	0	1	1	1	Exclusive OR
1	1	0	0	0	AND
1	1	0	0	1	AND
1	1	0	1	0	AND
1	1	0	1	1	AND
1	1	1	0	0	OR
1	1	1	0	1	OR
1	1	1	1	0	OR
1	1	1	1	1	OR

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6.12.3. Concentrator

The information taken from B0 (signals UCA0 - UCA7) before being transferred to the arithmetical unit are treated suitably in function of the type of operation to be performed.

- If the operation is of the logic type (OR, AND, ORE) or of a binary addition the information are transferred unchanged.
- If the operation is a subtraction (Binary or decimal) the information are inverted bit by bit: e.g.:
01100101 becomes 10011010.
- If the operation is a decimal addition a 6 is added to the 1st and the 2nd quartet without considering the carry-over between the two quartet.
E.g. : 0011 0110 becomes 1001 1100.

These operations are performed by a logic network called arithmetical unit concentrator.

The outputs of the concentrator UL00 - 07, drive, together with R000 - 07 and URPE the arithmetical unit.

6.12.4. Calculation and possible correction of the result

In order to perform the required operations, the commands CI45, CI46 and CI47 supply the decodings:

- (Ch 087-25) UC001=1 if decimal addition
- (Ch 087-30) UC011=1 if decimal or binary subtraction
- (Ch 087-33) UC021=1 if binary addition or logic operation
- (Ch 090-3) UC031=1 if AND or OR operation
- (Ch 087-24) UC041=1 if OR or ORE operation
- (Ch 090-1) UBI01=1 if not decimal operations.

Operating on data arriving from R0 and from the concentrator, the arithmetical unit supplies:

- the AND bit by bit of the two operands (signals UN00 - 07)
- the ORE bit by bit of the two operands (signals UB00 - 07)
(the OR is not calculated, but it is obtained as the sum of the AND and of the ORE)

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- the addition of the two operands through a binary adder having the outputs US00 - US07.

In the case of subtraction, the addition of the two operands is in reality the difference -1 as the 2nd operand has been inverted.

If the incoming carry-over (URPE) is "1" there is the real difference.

The results of the addition of the individual bits are generated considering the results of the AND and of the ORE of the bit under exam and the possible carry-over of the less significant bits.

It is to be noted that URPE may condition also the 1st bit of the 2nd quartet (US04). This occurs when the command CI51 that means URPE in UA2 is issued from sequence.

The results of ORE, AND, and binary addition go to the output of the UA where, in function of the operation required, the result is generated.

In case of decimal addition or subtraction, the result is generated considering the logic level of the carry-over of the quartet under exam (URO3 and URO7).

If the carry-over is "0" the result is added to 10. This operation is called decimal correction.

Should the information taken from B0 contain not numerical configurations, it is then necessary to stop the decimal correction.

For this purpose, if the outputs UL00 - 07 of the concentrator were having in one of the two quartets the configurations:

0000
0001
0010
0011
0100
0101

it means that before the +6 addition or before the inversion the information had a not numerical configuration.

The decoding of these configurations provides to force to "1" URO3 or URO7 through the signals UDC11 (090-21) or UDC21 (093-21), this operation stops the decimal correction.

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The carry-over in output (URPU) is normally loaded with the carry-over of the 8th bit URO7. If the sequence issues the command CI50, it is loaded instead by the carry-over of the 1st quartet URO3. The loading of URPU is in addition conditioned to the fact that the cycle performed was of CPU, to avoid that a channel 2 operation clears URPU.

6.13. Check network and errors

The check network calculates, for every configuration present in the RO register, the related odd parity bit. The signal GECE1 (085-22) represents the calculated check and is used to establish the value of the check bit to be written in memory with the suitable conditions.

The signal GECE1 is compared with the value of the bit R008 and in case of disparity between the calculated check and the check present in R008 the signal GEST1 (085-23) goes to "1".

The signal GEST1 is used to detect with suitable conditions the occurrence of a memory internal error or the occurrence of a disparity error on the data arriving from the peripheral units.

6.13.1. Check bit issue

The signal R008 (086-21) represents the disparity bit which must be written in memory.

If the FF GE00 (086-20) is set, the check calculated by the check network (GECE1) is written in memory.

If the FF GE00 is reset, the value of the bit R008 is written in memory.

The FF GE00 is set by every pulse T020.

Every time a reading from memory (C030D=0) is performed, it is reset by the pulse T050 to re-write the check read (GESOA=0, 086-19).

When a recording in memory is performed, the signal GESOA goes to "1", and resets GE00, (it does not allow the recording of the calculated check) only when the signal GESI1 (086-24) goes to "0".

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GESI1 goes to "0" when:

- the key INCE (ACECB=1) is inserted and the command CI341 (NE in R0) is present;
- the key INCE is inserted, and the rotary switch is not in normal position (AF32D=1).

6.13.2. Internal error

The internal error is stored in the FF GERI (086-4) when all the following conditions are verified:

- the check network has detected a disparity error (GEST1=1);
- the memory reading command has been accepted (C0302=1);
- the memory address explored was valid (MEVA1=1).

The FF GERI is reset by the "Clear" key (signal ASGAF=0) or by the command C035 and set during the phase of the instruction JIE (jump on internal error).

6.14. Invalid address

When a reading or a recording in memory address a memory zone not existing or not enabled, the operation is the following:

- the starting of the memory Delay Line is stopped;
- the FF INVA (086-13) which switches on the related bit lamp on the operator panel is set;
- through INVAB=0 the CPU Delay Line recycle is stopped, if the maintenance panel INAR key is not inserted.

The FF INVA (086-13) is always set by the pulse T0202 every time a reading or recording command (INVS2=1, 086-22) is issued.

If the address is valid the signal VAMEA, beside starting the memory Delay Line, resets the FF INVA after about 100 ns, and therefore there is no signal.

In the opposite case, as the memory Delay Line must not start, there is no VAMEA, therefore the FF INVA stays set stopping the main timing.

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6.15. Pulse use

- T000 - Stores the asynchronous requests (FF RIA0, RESI, RIA2, RIA3, ch. 131)
 - Sets the RAMx time counter (ch. 133)
- T010 - Loads the RAMx time counter (ch. 133)
 - Stores the cycle attribution (ch. 132)
 - Loads the SA register (ch. 110)
 - Loads the FA register (ch. 112)
 - Enables the commands of the 1st phase for the NO knot and counting network selection (ch. 36 - 39)
 - Resets initially URPE (ch. 91)
 - Resets initially INVA (ch. 86)
 - Resets ACIC (recycle of Delay Line, ch. 22)
- T011 - Enables the set of FF RUF2 (ch. 143)
- T015 - Issues TU04 (ch. 145)
- T019 - Sets RAVI (VICU support, ch. 140)
 - Sets RACI (rejected command, ch. 140)
 - Sets RIGI (end from controller on channel 1, ch. 138)
 - Sets RIG3 (end from controller on channel 3, ch. 146)
 - Sets RILI (end from length on channel 1, ch. 138)
 - Resets RUF1 (FINU support, ch. 139)
 - Resets REN2 (pre-storage end of channel 1, ch. 139)
 - Resets RAN2 (pre-storage end of channel 3, ch. 147)
 - Stores the connector name (PRxx, ch. 134)
 - Resets RECE (selection check byte, ch. 135)
 - Sets RASI (transfer with channel 1, ch. 136)
 - Sets PUC2 (selection of channel 2, ch. 136)
 - Sets PIC3 (selection of channel 3, ch. 136)
 - Sets RUSC (data exchange in channel 3 output, ch. 148)
 - Sets RIND (counts for decreasing addresses on channel 3, ch. 148)
- T020 - Loads registers BO and VO (ch. 69, 71, 73, 75)
 - Resets register RO (ch. 81, 83, 86)
 - Enables 1st phase of NIKnot selection (set NIFA, ch. 116)
 - Sets ALAM (operator call, ch. 23)
 - Sets ADIR (inhibits stop, ch. 24)
 - Sets INVA (ch. 86)
 - Resets GECC (enables R008 to memory, ch. 86)

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- T025 - Starts memory Delay Line (VAMEA=0, ch. 80)
 - Sets PICI (selection of channel 1, ch. 136)
 - Sets PIPO (loads RE and RA, ch. 136)
- T030 - Enables commands of 2nd phase for NO knot selection (ch. 36, 37, 39)
- T040 - 1st registers loading:
 P0 and V1 (ch. 56, 59, 62, 65)
 V3 and V4 (ch. 46, 49, 40, 43)
 L2 (ch. 41, 44)
 V2 (ch. 57, 60, 63, 66)
- T050 - 2nd B0 loading (ch. 73, 75)
 - RO loading from NO or NE knots (ch. 81-84, 86)
 - Resets URPE and URPU (ch. 91, 94)
 - Sets PEC4 (resets channel 1, ch. 136)
 - Sets PEC1-3 (resets channels 1, 2, 3)
- T065 - Enables the 2nd phase commands for count selection (ch. 38)
 - Resets URPU and URPE (ch. 94 and 91)
 - Issues TU30 channel 1 (RT13, ch. 149)
 - Issues TU30 channel 3 (RT33, ch. 149)
 - Resets RILI (end from length on channel 1, ch. 138)
 - Resets RIGI (end from controller on channel 1, ch. 138)
 - Sets RUF1 (FINU support, ch. 139)
 - Resets REN2 (pre-stores end on channel 1, ch. 139)
 - Resets RIL3 (end from length on channel 3, ch. 146)
 - Resets RIG3 (end from controller on channel 3, ch. 146)
 - Sets RUF3 (end of transfer on channel 3, ch. 147)
 - Resets RAN2 (pre-stores end on channel 3, ch. 147)
 - Sets RICO and RICI (difference counter for MZ, ch. 142)
 - Sets RUF2 (end of transfer on channel 2, ch. 143)
- T070 - Enables the 2nd phase of the NI knot selection commands (ch. 116)
 - Resets URPU (ch. 94)
 - Resets ADIR (ch. 24)
 - Sets RECE (selection check byte, ch. 135)
 - Sets RER3 (disparity error in channel 3 input, ch. 147)
 - Sets RAN2 (pre-stores end on channel 3, ch. 147)
 - Sets RERI (disparity error in channel 1 input, ch. 139)
 - Sets REN2 (pre-stores end on channel 1, ch. 139)
 - Sets RICS (permission to issue TU04, ch. 145)

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- Resets PICI, PIC3 (channel 1 and 3 selection, ch. 136)
- Resets RASI (transfer on channel 1, ch. 136)
- Resets PEC4 (reset condition on channel 1, ch. 136)
- Resets PUC2 (channel 2 selection, ch. 136)
- Resets RUF2 (end of transfer on channel 2, ch. 143)
- Resets ERAR (disparity error of photodisc code, ch. 143)
- Resets REAB (MZ cycle requests, ch. 143)
- TO80 - Resets AVER (condition checked, ch. 24)
 - Sets ALTO (enables internal calculation, ch. 25)
 - Sets GERI (internal error, ch. 86)
 - Sets REN2 (pre-stores end on channel 1, ch. 139)
 - Sets RAN2 (pre-stores end on channel 3, ch. 147)
 - Resets RCOO-03 (stores requests, ch. 129, 130)
- TO89 - Resets ASTO (enables Delay Line recycle, ch. 22)
 - Resets AINI (program loading, ch. 23)
 - Resets ALAM (operator call, ch. 23)
 - Resets PEC1-3 (stores channels reset, ch. 137)
 - Sets ERAR (photodisc code error, ch. 143)
 - Sets RICI (difference counter for MZ, ch. 142)
 - Sets RINI, RINO (buffer to issue TU02, ch. 145)
- TO90 - Sets ACIC (main Delay Line recycle, ch. 22)
- TI05 - 2nd registers loading:
 - PO, V1 (ch. 56, 59, 62, 65)
 - V2 (ch. 57, 60, 63, 66)
 - L1 loading (ch. 57, 60, 63, 66)
 - PO loading (ch. 104)
 - Sets URPU (ch. 94)
 - Sets ACIC (lengthened recycle, ch. 22)
- TI06 - S1 loading (ch. 108)
 - FI loading (ch. 112)
 - SO loading (ch. 106)
 - 2nd registers loading:
 - V3, V4 (ch. 40, 43, 46, 49)
 - L2 (ch. 41, 44)
 - L3 loading (ch. 41, 44, 47, 50)
 - RI loading (ch. 47, 50)

Note: this pulse has the same timing of the previous one. The operations of these two pulses have been divided only for loading needs.

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- TI10 - Issue TU20 on channel 3 (RT32, ch. 147)
- Issue TU02 (trigger for integrated MZ, ch. 145)
 - Issue TU20 on channel 1 (RT12, ch. 139)
 - Issue TU10 on channel 3 (RT31, ch. 149)
 - Issue TU10 on channel 1 (RT11, ch. 149)
 - Sets RUCO, RUCI (TU04 issue counter, ch. 144)
 - Sets RINO, RINI (buffer to issue TU02, ch. 144)
 - Sets RATE (AEDE issue, ch. 141)
 - Sets FIRU (remove paper and stop, ch. 141)
 - Sets ARES (forces 8/0 in S0, ch. 22)

6.16.

Timing chart

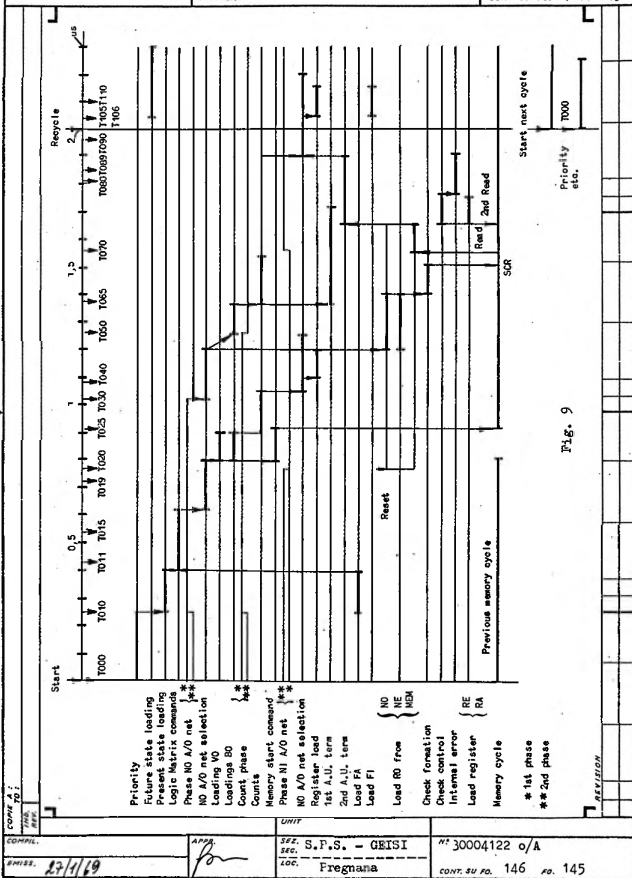
The chart on the following page gives the main CPU operations.

Naturally, even if the time relations between the various operations are complied with, these times are purely indicative.

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7. DETAILED DESCRIPTION OF MP AND DP SEQUENCES7.1. Multiplication7.1.1. General

Assume that the following operation is to be performed:
 748×425 (the first number is the MDO, the second is the MRE).

Generally, we would do this operation multiplying mentally the MDO by the figure indicating the units in MRE ($5 \times 748 = 3740$) then we multiply the MDO by the figure indicating the tens of MRE ($2 \times 748 = 1496$) setting this partial result under the 1st partial result moved of one position to the left, and so

7 4 8	MDO (Field 2)
4 2 5	MRE (Field 1)
<hr/>	
3 7 4 0	
1 4 9 6 0	
2 9 9 2 0 0	
<hr/>	
3 1 7 9 0 0	

Now let us try to do the same operation, starting from the most significant figure, instead that from the less significant figure of the MRE, i.e.:

7 4 8	MDO (Field 2)
4 2 5	MRE (Field 1)
<hr/>	
2 9 9 2 0 0	
1 4 9 6 0	
3 7 4 0	
<hr/>	
3 1 7 9 0 0	

obviously the result is the same.

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Now, instead of doing mentally the partial multiplications (4 x 748 etc...), let us divide these in additions:

0 0 0	
<u>7 4 8</u>	1
7 4 8	
<u>7 4 8</u>	2
1 4 9 6	
<u>7 4 8</u>	3
2 2 4 4	
<u>7 4 8</u>	4 End of MRE hundreds figure
2 9 9 2	
<u>7 4 8</u>	1
3 0 6 6 8	
<u>7 4 8</u>	2 End of MRE tens figure
3 1 4 1 6	
<u>7 4 8</u>	1
3 1 4 9 0 8	
<u>7 4 8</u>	2
3 1 5 6 5 6	
<u>7 4 8</u>	3
3 1 6 4 0 4	
<u>7 4 8</u>	4
3 1 7 1 5 2	
<u>7 4 8</u>	5 End of MRE unit figure
3 1 7 9 0 0	Final result

This is, in broad lines, how the machine works.

With reference to the Flow given in Fig. 10, the states F3/F2 - F8/F9 are defined as "OUT OF CYCLE", while the states 60/63 - 58/59 - 50/53 - 40/43 are defined as "CYCLE".

The status 7A/7B is a connection status.

As it is known, every memory position, as we are here dealing with packed numerical data, contains two figures;

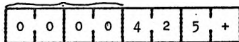
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the most significant figure will be called EVEN (position) figure, the other ODD (position) figure.

So when an EVEN FIGURE of MRE is examined, we will talk of EVEN OUT OF CYCLE and EVEN CYCLE; the same will be for an ODD FIGURE.

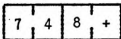
Here below, there is a diagram of the process, which takes into account the operands format:

L2+1 pos.
to zero



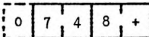
MRE Field

NORMAL Alignment



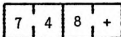
the 4 is
examined

OFFSET Alignment



the 2 is
examined

NORMAL Alignment



the 5 is
examined

In NORMAL alignment the various additions (in CYCLE) are performed between one position MDO and one position of MRE in the same order as they are in memory; e.g.:



(MRE)

with



(MDO)

In OFFSET alignment to the contrary, in correspondence of every position of MRE there are two semi-bytes of two different consecutive MDO positions.

For example:



(MRE)

with



(MDO)

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as indicated these two figures occupy two consecutive Memory positions.

Therefore, in the operation performance, in the ODD cycles, two consecutive positions of the MDO field should be read; the less significant semi-byte of the position more to the left is kept (in our example: 4), and the most significant semi-byte of the other position (in our example: 8) will be kept. Obviously, in the OFFSET alignment, the MDO is increased to the left with a zero semi-byte.

7.1.2. Multiplication phases

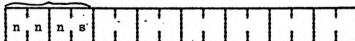
7.1.2.1. Preparatory phase

The performance of the multiplication is divided in three phases: the first is the so called preparatory phase, the second is the test phase, the third is the real performance.

In the preparatory phase provisions are made for:

- checking that 2 out of 3 conditions be respected which otherwise would generate overflow and precisely: $L_1 > L_2$, $L_2 \leq 7$;
- trasferring the MDO in a specialized memory zone: the most significant character to the address 232 (00E8 in hexadecimal) and the others at the following addresses according to an increasing order (states 20/21 - 28/29);

M D O

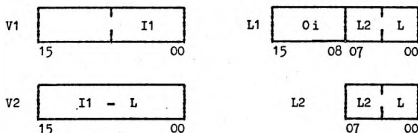


232 232 239
+L2

- setting the FF FI01; sign of the MDO positive: set FI01=1; if the sign of the MDO is negative, set FI01=0 (Status 20);
- setting the FF FI00 if there are some overflow conditions and going to phase α without starting the operation (status 23).

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At the end of the preparatory phase, the registers V1, V2, L1, L2 contain the following information:



where $L = L1 - L2$.

The FF SC00 at level "1" ends the preparatory phase.

7.1.2.2. Test phase

The test phase consists of checking that the L2+1 positions more to the left in the MRE field contain some zeroes. This check is performed in the following way: a subtraction is performed between the content of the L2+1 positions which must all be to zero and a fictitious field equal to all zeroes and having the same length; this operation is done without setting, initially, the FF URPE, therefore, because of the operation mode of the arithmetical unit, if the field under exam contains all zeroes, at the end URPU will be equal to zero, to the contrary URPU will be equal to 1; in this last case at the end of the test (7B) phase α is reached giving signal of overflow.

The states interested are: 61 - 59 - 51 - 41; if $L2 > 0$, the cycle 63 - 5B - 53 - 43 will be performed L2 times; then the status 7B is reached, from here, if there has been the overflow signal, the phase α is reached; to the contrary, the status F3 is reached (1st status of the EVEN OUT OF CYCLE).

7.1.2.3. Phase of the execution

We are giving here first a description of the use of the registers and the FF.

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- V1 : in cycle: it is loaded with the content of V2 (MRE digit address under exam) then it scans in the decreasing direction the MRE field as the partial result is recorded.
- Out of cycle: it is not significant.
- V2 : in cycle: it is positioned at the beginning of the MRE, i.e. it holds the address of the MRE digit under exam.
- Out of cycle: it undergoes a counting +1 at every EVEN OUT OF CYCLE (status F3).
- L1 : input to the even cycle:

X	X	L2	MRE even cycle
---	---	----	----------------

output from the even cycle:

partial	result	X	X
---------	--------	---	---

input to the out of cycle:

O _i	L2	X
----------------	----	---

input to the odd cycle:

partial result	O _i	L2	MRE odd cycle
----------------	----------------	----	---------------

output from the odd cycle:

partial	result	X	X
---------	--------	---	---

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- L2 :

L2	L
----	---

L2₁ undergoes a counting at every odd out of cycle. When it becomes zero, the operation is over.

- Condition Flip-Flop:

FA04: at the output of the preparatory phase it is at "0" (reset in the status 20): it distinguishes the first odd cycle, i.e. the TEST.

When it is at level "1" it means that the TEST is over (set in the status F8/F9).

SA00: a) in cycle: when it is at "0", it performs the EVEN cycle, i.e. a MRE EVEN digit is examined. When it is at "1" an ODD cycle is performed.

b) out of cycle: when it is at "0" an ODD OUT OF CYCLE is performed, i.e. the ODD DIGIT of MRE is examined; in status F2 the length of the operation L contained in the less significant part of L2 is decreased of 1. When it is at "1" the EVEN OUT OF CYCLE is performed, i.e. the EVEN DIGIT of MRE is examined; in the F3 status +1 is counted on the V2 addresser which is pointing on the MRE position under exam (set and reset by counter in the FA/FB status).

c) in preparation phase: when it is at "0" it defines the reading of the less significant position (i.e. the one of the MDO sign).

SA01: in cycle: when it is at "0", it establishes for every unit of the MRE digit under exam, the first addition cycle (set in the status 40 - 41, reset in the status 7A/7B).

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FA00: in preparation phase: if it is at "1" an overflow has occurred.

in cycle: if it is at "1", the units of the Multiplier under exam are finished (set in the status 40/43, reset in the status F8/F9).

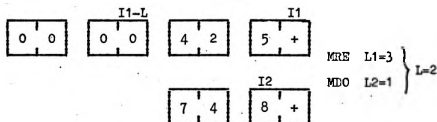
FA03: in cycle: when it is at "1" it indicates that the length of the MDO has finished (set in the status 60/63; reset in the status 7A/7B).

FA01: in preparation phase: at "1", it indicates $MDO > 0$ (set in the status 20).

out of cycle: at "1", it indicates a result greater than 0 (Status FA).

Now let us get back to our example of multiplication:
 748×425 ($748 = MDO$, $425 = MRE$).

The operands in memory will thus consist of:



After having performed the TEST, the status F3 is reached. Here V2 counts +1, i.e. it positions itself at the address $I1 - L + 1$ ($= I1 - L1 + L2 + 1$): i.e. the one of the first significant position of the MRE; in FB the following position is read



the most significant part (EVEN DIGIT) is put in LI1, the other part (ODD DIGIT) in LI3.
 A zero is put in LI4; in LI2 there is the length of the MDO L2, loaded previously in the 7B status.

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Note: this occurs if the EVEN DIGIT $\neq 0$, otherwise LI is left as it was at the output from the 7B status; i.e. LI₄₃ contains zeroes, LI₂ contains LI₂, LI₁ contains zeroes.

Then the status F8 is reached where the higher part of LI is written in memory at the address (I1 - L + 1), i.e.:

0	2
---	---

The EVEN CYCLE is thus started.

In 60 there is in 232 + L₂ the less significant position of the MDO (the one with the sign)

8	+
---	---

and it is set in LI₄₃; L₂ is decreased and if this one is equal to zero, FIO₃ is set.

In 50 there is the MRE position

0	2
---	---

with V₂, and the addition (limited to the most significant two semi-bytes only) is performed

0	2
---	---

+

8	+
---	---

and the result is set in LI₄ (in LI₃ the 2 is by-passed). A decount is made on LI₁, i.e. EVEN DIGIT of MRE; V₁ is loaded with the content of V₂.

In the status 40 the content of LI₄₃ is recorded at the address I1 - L + 1 (V₂).

If the MRE EVEN DIGIT in LI has become zero, FIO₀ is set. A decount is made on V₁.

At this point, if L₂ is not over (i.e. MDO has more than one position) or if the previous addition has given a carry-over the previous cycle is repeated but from now on the states 62 - 52 - 42 will be done.

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When, to the contrary, L₂ is over and the last addition has not given carry-over, the status 7A is reached. Here, the L₂ is reset in LI₂, FIO₃ is reset, O_i are forced in LI₄₃; then, if the number of the Multiplier under exam has passed to zero (i.e. LI₁ = 0 : FIO₀ = 1) the status F₂ is reached (start ODD OUT OF CYCLE); otherwise the status 60 is reached again and the above mentioned cycle (60 - 40 - 50 - 62 - 52 - 42 - 7A etc.) is repeated until the EVEN DIGIT is finished. In F₂ (start of ODD OUT OF CYCLE) L is decounted (in L₂). In FA, as V₂, after the F₃ status, has not changed, the reading is still at the address I₁ - L + 1; this time, the memory position contains: the digit unit of partial result in the most significant semi-byte and the ODD DIGIT of MRE or the sign when L = 0 (in our case):

2	2
---	---

The ODD DIGIT is set in LI₁, in LI₃ a zero is set while the digit of the partial result passes in LI₄. All this occurs only when there is L=0 or ODD DIGIT ≠ 0; to the contrary LI would not be modified.

In the case in which L = 0, in the status FA, the sign of the result, too, is generated according to the algebra rules.

The status F₉ is then reached in which, if L = 0, the sign of the final result is forced and the qualitatives are set.

If L ≠ 0, the content of LI₄₃ is written in the MRE field

Partial result,	0.
--------------------	----

i.e. the ODD DIGIT of the MRE under exam is cleared.

In addition, the FF FIO₀ is reset.

The ODD CYCLE is thus started.

In 61 the MDO less significant position is read in 232 + L₂

8	+
---	---

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the most significant digit (8) is set in LI_3 . L_2 is decounted, and if this is equal to zero, it set FIO_3 . In 59 the reading is done at $232 + L_2 - 1$, i.e. in one position more to the left than the previous one.

7	4
---	---

the less significant digit (4) is set in LI_4 . At this point LI_{43} contains

4	8
---	---

In the case when $FIO_3 = 1$ (MDO over) it is not read and a zero is set in LI_4 . In the 51 status the MRE position addressed by V2 is read

Partial result,	0
-----------------	---

and it is added to the content of LI_{43} unloading the partial result in LI_{43} . A decounting is done on LI_1 (MRE ODD DIGIT under exam). V2 is unloaded in V1. The 41 is reached in which the content of LI_{43} (partial result) is written in the field of the MRE at the address contained in V2. A decounting is made on V1. At this point if $FAO_3=0$ or $FAO_3=1$, but the previous addition has given a carry-over, the cycle is performed again: but from now onward the states 63 - 5B - 53 - 43 will be performed. If instead $FAO_3=1$ and the carry-over is equal to zero, the 7B is reached. Here, L_2 is reset in LI_2 , FIO_3 is reset, O_i is forced in LI_{43} then, if the MRE ODD DIGIT under exam is gone to zero (i.e. $LI_1 = 0$ $FIO_0=1$) the status F3 is reached (beginning of EVEN OUT OF CYCLE) otherwise the status 61 is reached again and the above mentioned cycle 61 - 59 - 51 - 41 - 63 - 5B 7B etc. . . . is repeated until the ODD DIGIT is finished. The above mentioned mechanism (EVEN OUT OF CYCLE - EVEN CYCLE - ODD OUT OF CYCLE - ODD CYCLE) is repeated until arriving at the F2 status, V2 is found set on the posi-

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tion containing the sign; L is decounted and it goes to zero.

In the FA status the position containing the sign and the UNIT digit of the final result is read: this last one is set in LI₄ while in LI₃ a zero is set.

The sign is examined and FIO1 is set.

In the F9 status, the sign of the result is forced ("C" if "+" sign, "D" if "-" sign) in memory. The qualitatatives are set and phase α is reached.

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7.1.3. - Multiplication flow

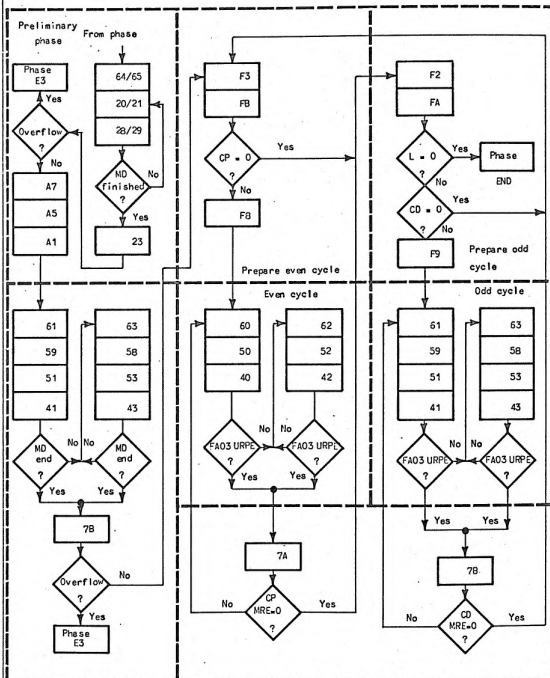


Fig. 10

7.2. Division

It is assumed that the Multiplication is known.

7.2.1. General

As for the Multiplication let us give an example first.
Assume that the following operation is to be performed:
49258 : 367 = 134 (1st operand: DDO - 2nd operand: DRE).
Here below is how this operation is generally done:

$$\begin{array}{r} 49258 : 367 = 134 \\ 1255 \\ 1548 \\ 80 \end{array}$$

We examine (starting from the most significant) as many digits of the DDO as the ones of the DRE; we calculate the number of times the DRE may be contained in the group of digits considered: this number (which may also be zero) forms the first digit of the Quotient (in our case $492 : 367 = 1$).

If the DRE is not contained exactly in the considered DDO part, the remained is written (in our case 125). Then the number formed by the remained and the digit following the group considered is examined (in our case 1255): we calculate how many times the DRE may be contained in this new number; this number if the second digit of the quotient (in our case $1255 : 367 = 3$). And so on until the last digit of the DDO has been considered.

The last remainder obtained is the remainder of the division (in our case 80).

Let us now divide the calculations that we have performed with many elementary subtractions:

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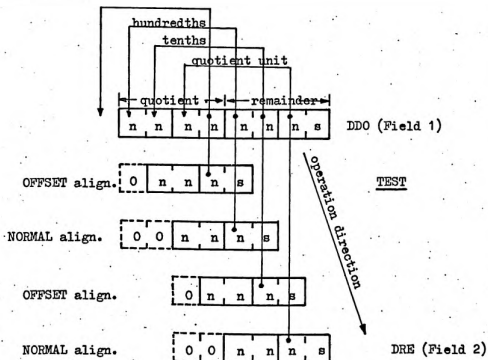
	49 25 8+		DDO (Field 1)
	<u>36 7+</u>		DRE (Field 2)
	12 5	1	1st subtraction
	<u>36 7</u>		2nd subtraction
Negative carry over	75 8	2	addition
	<u>36 7</u>		
	12 55	1	1st quotient digit
	<u>3 67</u>	1	
	08 88		
	<u>03 67</u>	2	
	05 21		
	<u>03 67</u>	3	
	01 54		
	<u>03 67</u>		
Negative carry over	97 87	4	addition
	<u>03 67</u>		
	01 54 8	3	2nd quotient digit
	<u>36 7</u>		
	01 18 1	1	
	<u>36 7</u>		
		
		
	00 08 0		
	<u>36 7</u>		
Negative carry over	99 71 3	5	addition
	<u>36 7</u>		
Remainder	08 0	4	3rd quotient digit

↑
Evolution of the quotient digits

The machine operates more or less as described above, i.e. for a certain alignment the DRE is subtracted from the DDO field until this has become smaller than the DRE itself: there is a negative carry over and a partial result complemented in field 1; it is therefore necessary to add once the DRE to field 1 in order to re-establish the normal operation.

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Then, the DRE is moved of one semi-byte to the left and the same subtraction cycle is repeated. This until the DRE unit digit is aligned under the DDO unit digit. As far as the operands length is concerned, it is necessary to point out something. As already mentioned, the Field of the DDO must have a length such as to contain the remainder ($L_2 + 1$ positions) and the quotient. In our case, the remainder will occupy two positions and the quotient, too, then field 1 has to have 4 positions; therefore there is the need to add to the left of the 1st significant digit of the DDO a position containing all zeroes. All this will be better explained at paragraph 7.2.3. talking of the TEST.



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As far as the definitions of OFFSET and NORMAL alignment are concerned refer to the multiplication description. The dotted rectangles to the left of the DRE mean that, during the operation, to the DRE one or two "zeroes" will be "added".

Here too, similarly to the Multiplication, we speak of ODD and EVEN CYCLES and OUT OF CYCLES, considering as EVEN those cycles and out of cycles in which the unit digit of the DRE is aligned under an EVEN (in position) digit of the DDO; similarly as far as the ODD definition is concerned.

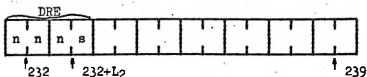
7.2.2. Division phases

The performance of the division is divided in three phases: preparatory, test, and execution.

7.2.2.1. Preparatory phase

This phase provides to:

- check that at least two of the four conditions which would otherwise cause overflow, and precisely $L_1 > L_2$, $L_2 \leq 7$ (states 28/29) be complied with;
- transfer the DRE in a specialized memory zone: the most significant character to the address 232 (OOE8 in hexadecimal) and the others, at the following addresses in an increasing order (states 20/1 - 28/29);



- set the FF FIO1: if the sign of the DRE is positive, set FIO1=1; if negative, set FIO1=0 (status 20);
- if there are overflow conditions, set the FF FIO0 and go to phase α without starting the operation (status 23).

At the end of this phase, the registers V1, V2, L1, L2 contain the following information.



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I1 - L
15 00

V2

L2	L
07	00

L2

where $L = L_1 - L_2$.

Finally, the FF S000 at "1" ends the preparatory phase.

7.2.2.2. "Test" phase

The test consists of the check that the DRE be different from zero, and that the field 1 (DDO) be long enough to contain the remainder and the quotient which will be arranged in field 1 in the following way:

N1 positions			
quotient		S	remainder S
N1-N2			N2

$$L_1 = N1 - 1$$

$$L_2 = N2 - 1$$

Therefore the quotient will have to be, at the maximum, of $[2(N1 - N2) - 1]$ digits (plus the sign). Refer to the diagram of page 161.

The quotient sign will occupy the less significant digit of the $(N2+1)$ -th position of field 1 starting from the right; i.e. it will occupy the $(2 \cdot N2 + 1)$ -th digit. The first digit of the quotient (unit digit) will occupy the $(2 \cdot N2 + 2)$ -th digit of field 1. And so on.

The unit digit of the quotient will be generated when the unit digit of the DRE is aligned under the unit digit of the DDO; the tens digit of the quotient will be generated when the unit digit of the DRE is aligned under the tens digit of the DDO. And so on for the other digits. Therefore it can be said that a quotient digit is generated for every different alignment.

The consequence is that, as there should be $[2(N1-N2) - 1]$ digits in the quotient, the number of the alignments will be the same; as a consequence the alignment corresponding to the generation of the most significant digit of the quotient (i.e. the digit $2 \cdot N1$ of field 1) will be the one in which the unit digit of the DRE is under the $2(N1 - N2)$ -th digit of field 1. (Refer also to diagram on page 161).

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As a consequence, aligning the DRE so that its unit digit be under the $[2(N_1 - N_2) + 1]$ -th digit of field 1, and subtracting the DRE from the DDO, the result should be that the DDO be $<$ of the DRE: in the opposite case, in fact, an additional digit of the quotient will have to be generated outside field 1. The TEST consists of this.

According to the performance of the Arithmetical Unit, if the DDO (1st operand) is $<$ than the DRE (2nd operand), the final carry-over will have to be zero; if, instead, DDO is $>$ of DRE or DDO = DRE the carry-over will be equal to 1. It is natural that the DRE is zero the carry-over will always be equal to 1 also in the case in which the DDO, too, be equal to zero.

The states interested are: 61 - 59 - 51 - 41; if $L_2 > 0$ the cycle 63 - 5B - 53 - 43 is performed L_2 times; then the status 7B is reached; here, if there has been an overflow (URPE = 1) phase α is reached; in the opposite case, the status F3 (1st status of the EVEN OUT OF CYCLE) is reached. The test does not change the content of field 1. (in fact, during the status 40 - 43 a recording is made only if FA04 = 1).

Note 1: The alignment of the TEST is therefore the one in which the unit digit of DRE is under the less significant digit of the position of DDO with address I1 - (N1-N2). (We will see in the preparatory phase that this address will be loaded in the register V2).

Note 2: The starting alignment may also be defined as the one in which the first digit (from the left) of the DRE is under the second (from the left) digit of the DDO. It is important to point out that what has been mentioned is valid independently from the two lengths L_1, L_2 .

Note 3: It is obvious, as per what mentioned sub note 2, that, if the first digit (from the left) is different from zero, there will be an overflow.

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In fact, assuming that the first digit be 2,
the two operands would be:

2	X	X	X	X		1
0	X	X	X			2

obviously the 1st operand > 2nd operand.

Note 4: In the case that the absolute values of the DDO and DRE are not known, the mathematic certitude that the quotient may be contained in field 1 (together with the Remainder) is obtained only if it is possible to have in field 1 (starting from the left) as many positions to zero (consecutive) as there are in the DRE.

7.2.2.3. Performance phase

We are giving first a definition of the use of registers and Flip-Flops.

- V1 a) in cycle : it is loaded with the content of V2 in the status 50-51, then it scans, in a decreasing sense, the field of the DDO as the partial result is recorded in it. It is decoupled in the status 40/43.
- b) out of cycle: in the out of cycle the memory position (field DDO) in which the calculated quotient digit must be recorded is addressed.
- V2 a) in cycle: it contains the address of the DDO digit aligned with the UNIT digit of the DRE.
- b) out of cycle: it undergoes a counting +1 at every EVEN OUT OF CYCLE (status F3).
- L1 a) input to the EVEN cycle:

X	X	L2	Oi
---	---	----	----

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b) output from the EVEN cycle:

X	X	14	Quotient digit
---	---	----	-------------------

c) input to the EVEN OUT OF CYCLE:

X	Odd digit quotient	L2	Quotient digit
---	-----------------------	----	-------------------

d) input from the ODD OUT OF CYCLE:

Quotient digit	X	L2	Quotient digit
-------------------	---	----	-------------------

e) input to the ODD cycle:

X	X	L2	01
---	---	----	----

f) output from the ODD cycle:

X	X	15	Quotient digit
---	---	----	-------------------

- L2

L2	L
----	---

L2, undergoes a counting at every ODD OUT OF CYCLE; when it becomes zero, the operation ends.

- Flip-Flop of condition:

FA04 - during the preparatory phase it is reset (status 20). It determines the first odd cycle, i.e. the TEST.

When it is at level "1" it means that the test is over (set in the status F8/F9).

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- SA00 - a) in cycle: when it is at "0", an EVEN cycle is performed, i.e. the alignment is NORMAL. When it is at "1" an ODD cycle is performed, i.e. the alignment is "OFFSET".
- b) out of cycle: when it is at "0", an ODD OUT OF CYCLE is performed. When it is at "1" an EVEN OUT OF CYCLE is performed. (set and reset by counter in the FA/FB status).
- c) in preparatory phase: when it is at "0" it determines the reading of the less significant position (the one of the sign) of the DRE.
- SA01 - a) in cycle: when it is at zero it determines, for every digit unit of generated quotient, the first cycle of subtractions (or additions, after having had a negative carry-over). (Set in states 40-41, reset in the status 7A/7B).
- FA00 - a) in preparatory phase: if it is at "1" an overflow has occurred.
- b) in cycle: it is set (in the status 7A/7B) when the last cycle of subtractions has given a negative carry-over, i.e. the DDO has become smaller than the DRE. After that the DRE must be added once to field 1 to re-establish normality. In the status 50 or 51, with FA00=1 "+1" will be decoupled on the quotient digit generated up to that moment; with FA00=0, instead, +1 will be counted. (It is reset in the status FB/F9).
- FA03 - a) in cycle: when it is at "1" it indicates that the length of the DRE is finished (set in the status 60/63; reset in the status 7A/7B).
- FA01 - a) preparatory phase: at "1" it indicates $DRE > 0$ (set in the status 20)
- b) out of cycle: at "1" it indicates a result greater than 0 (status FA).

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Let us go back to our example of division:

49258 : 367 = 134 remainder 80.

As already mentioned, it is necessary to set one position to zero to the left of our real DDO in field 1.

Field 1
(beginning)

								I1	
0	0	4	9	2	5	8	+	DDO	

				Quotient	Remainder I1			
end	1	3	4	+	0	8	0	+

Field 2
(beginning)

				I2	
3	6	7	+	DRE	

				I2	
3	6	7	+		

$L_1 = 3$ $L_2 = 1$ $L = L_1 - L_2 = 2$

$I_1 = 1000$ $I_2 = 2000$

The test consists of the subtraction of

0	3	6	7	from	0	0	4	9
---	---	---	---	------	---	---	---	---

It is reached from the preparatory phase having $SOO0 = 1$, then the status 61 is performed. Here, the less significant position of DRE is read (at the address 232+1):

7	+
---	---

from which the most significant digit is lowered in LI_3 . (OFFSET alignment).

A decout is made on the length of the DRE contained in LI_3 . In the status 59 the 2nd DRE position is read (at the address 232)

3	6
---	---

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and its less significant digit is lowered in LI₄, so that now in LI₄₃ there is:

6	7
---	---

The status 51 is reached where the DDO position addressed by V2 is read (I1 - L = 998), i.e.

4	9
---	---

the following subtraction is performed

4	9	-	6	7
---	---	---	---	---

and the result is unloaded

8	2
---	---

in LI₄₃. (+1 is counted on LI₁; but this does not have any importance during the test). V1 is loaded with with the content of V2 (998). In the status 41, V1 is decounted and FIO0 is set. As the DRE length is not over yet (FIO3 = 0) the status 63 is reached where at address 232 is read:

3	6
---	---

the most significant digit (3) is set in LI₃; a decounting is made on LI₂ which goes to 15. FIO3 is set (DRE length over). In the status 5B the reading is not done from memory and a zero (RO₁) is lowered in LI₄. LI₄₃ now contains

0	3
---	---

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The status 53 is reached where the DDO (with V1) is read

0	0
---	---

and the subtraction is performed

0	0
---	---

-

0	3
---	---

the result

9	6
---	---

is unloaded in L1₄₃. In the status 43, a recording is not made, V1 is decremented (997 - 1 = 996). When FA03 = 1, the status 7B is reached (in the opposite case, the cycle 63 - 5B - 53 - 43 will be repeated until L₂ is finished); in this status in L1₂ the length of the DRE is reset, FIO3 is reset. In our example, as URPU = 0, the status F3 (EVEN OUT OF CYCLE) is reached; in the opposite case, phase α will be reached giving an overflow signal. End of Test.

Status F3. +1 is counted in V2 (999) and L1₁ is cleared (in cycle it will contain the Quotient digit).

Status FB. It is not read because FA04 = 0, then a zero (RO₂) is unloaded in L1₄ but this is not important for the following:

L1

X	X	L2	0
---	---	----	---

Status FB. A writing is not performed because FA04=0; the only significant operations are the set of FIO4 and the reset of FIO0.

The EVEN cycle is started. Field 1, let us remember it, has undergone no variations yet.

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Status 60. The DRE is read at $232 + 1$

7	+
---	---

and this position is unloaded in $L1_{43}$ (NORMAL alignment).
A decoupling is made on L_2 ($1 - 1 = 0$).

Status 50. The DDO is read with V_2 (999);

2	5
---	---

the subtraction is performed

2	-	7
---	---	---

(the most significant part only is processed, RO_1 is by-passed in $L1_3$) and the result is unloaded in $L1_4$.

5

+1 is counted in LI_1 : first unit of the quotient digit ($0 + 1 = 1$).

$L1$:

5	5	0	1
---	---	---	---

V_2 is unloaded in V_1 (999).

Status 40. $L1_{43}$ is written at the address contained in V_1 (999), a decoupling is made in V_1 ($999 - 1 = 998$).
At this point if $L1_2 = 14$ ($L104=0$), the status 7A would be reached, otherwise, and it is our case, the status 62 is reached performing then, as we will see, the states 52-42. The cycle 62-52-42 is performed ($L_2 + 1$) times.

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Status 62. The DRE position in 232 is read.

3	6
---	---

and is lowered as it is in L143, a decounting is made on L2 (0 - 1 = 15); FIO3 is set.

Status 52. The DDO is read with V1 (998)

4	9
---	---

the subtraction is performed:

4	9	-	3	6
---	---	---	---	---

the result

1	2
---	---

(the previous subtraction had given a negative carry-over) is unloaded in L143. Obviously, a counting is not done in L1;

L1 :

1	2	15	1
---	---	----	---

Status 42. L143 is written at the address contained in V1 (998), V1 itself is decounted (998 - 1 = 997).

The subtraction is not complete, in fact it is necessary to update again the position of DDO at the address 997. Therefore the cycle 62 - 52 = 42 is reached again and there this subtraction is performed:

(DDO)

0	0
---	---

 -

0	0
---	---

 (DRE) =

0	0
---	---

(to be noted that in 42, V1 is not decounted).

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At the end of the status 42, the field of the DDO is thus modified:

0	0	1	2	5	5	8	+
---	---	---	---	---	---	---	---

V1 contains 997, V2 contains 999, FA00 = 0 (because URPE = 1).

The status 7A is then reached in which L2 is reset in L12, L11 is transferred, (quotient digit generated up to this moment, in our case: 1) in L14, FIO3 is set. Then the cycle 60-50-40-62-52-42-62-52-42 is performed again; this time 7A is reached with URPE=0, in fact the subtraction has been performed:

00	12	5	-	00	36	7	=	99	75	8
----	----	---	---	----	----	---	---	----	----	---

with URPE=0 as subtrahend < minuend.

This last condition sets the FF FIO0; but FA00 at the end of the status is still at "0" and therefore the cycle 60-50-40-62-52-42-62-52-42 is performed again; this time, though, to the contrary of the other times, (in which there was FA00=0) in the 50 (and 52) status the additions are done instead of subtractions and the quotient digit is decremented of 1 (in L11) generated up to that moment. In particular in our case, the final digit of the quotient will be 1.

The status 7A is then performed in which among the other operations L11 (quotient digit = 1) is transferred in L14 and then the status F2 is reached (ODD OUT OF CYCLE). It is necessary to remind here that V1 contains the address 997, V2 contains 999, L21 contains 2.

Status F2. It is decremented in L21 (2 - 1 = 1) and L11 is cleared, where, in cycle the new quotient digit will be generated.

Status FA. The memory is read with V2 (999) but this is not significant in this moment; it will be significant only when the last position of the DDO field will be read, i.e. the one containing the sign.

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Status F9. In this status the quotient digits in EVEN position contained in L1₄ are written

1	X
---	---

(in our case)

at the address contained in V1 (997), F100 is reset. The last time that this status is reached, i.e. when L2₁ = 0, beside the odd digit, the quotient sign is written.

At this point, the cycle 61-59-51-41-63-5B-53-43 subtracting once the DRE from field 1. (We are not here repeating the explanation, status by status, already done at the beginning of our example). The result is 08 88 with URPE=1, then after the status 7B is performed a re-cycle is made to perform 61-59 ... 43 subtracting for a second time the DRE (the quotient digit is always filled out in L1₁) obtaining as a result 05 21 with URPE = 1; 7B is performed again and the cycle 61 ... 43 is performed for the third time obtaining 01 54 with URPE = 1. The fourth time 97 87 is obtained with URPE=0, then, after 7B has been performed (in which F100 is set) the cycle is reached again but this time in 51 (53) the additions, in place of the subtractions, are performed and the quotient digit in L1₁ is decreased (instead of increased) by 1. 7B is reached again (as always) L₂ is regenerated in L1₂; and the (ODD) digit of the quotient is transferred from L1₁ to L1₃.

At this point V2 contains 999, V1 contains 997 L2₁ contains 1.

Then the EVEN OUT OF CYCLE is performed.

Status F3. +1 is counted in V2 (999 + 1 → 1000) and L1₁ is cleared.

Status FB. The memory is read with V1 (997):

Even digit	1
quotient	0

and R0₂ is transferred in L1₄, i.e. the EVEN DIGIT of the Quotient previously generated is maintained.

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Status F8. L1₄₃ is recorded

Odd	Even
Digit	Digit

(in our case

1	3
---	---

in field 1 (997)). F100 is reset.

At this point an Odd Cycle (already described) is performed again, obtaining as quotient digit the digit 4 and as remainder in the field of the DDO 08 04.
After the status 7A, V2 contains 1000, V1 contains 998, L1₁ contains 4, L2₁ contains 1.
The the last ODD OUT OF CYCLE is performed.
A decoupling is made during F2 on L2₁ ($1 - 1 = 0$: end of the operation) and L1₁ is cleared.

Status FA. The memory is read with V2 (address 1000): position of the DDO sign; the sign itself is examined and the FF F101 is set accordingly.

Status F9. The sign is forced in R0₁ and it is recorded in memory with the EVEN digit of the quotient contained in L1₄.

4	+
---	---

at the address of V1 (998). The qualitatives are position ed and thus the operation is ended.

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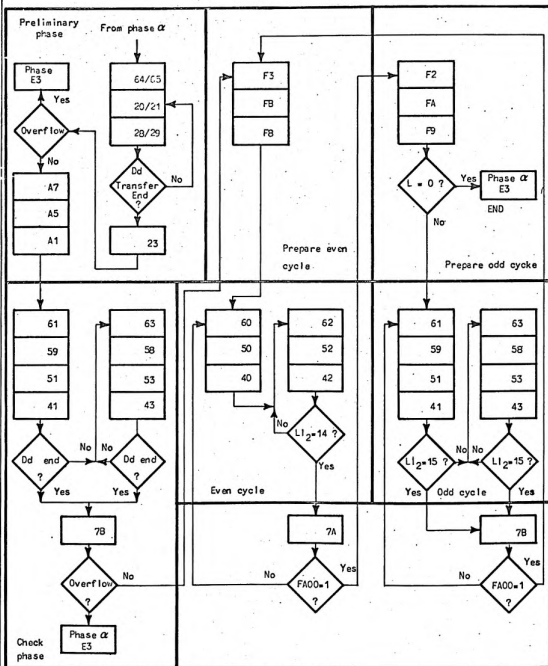


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8. DETAILED MEMORY DESCRIPTION8.1. General

The memory has a capacity which can vary from 8K to 32K positions which can be addressed individually. In the case of maximum capacity the memory pack contains 40 boards and 2 matrixes.

The memory is located in the lower part of the Central Processor wing because of ventilation problems.

8.2. Description of block diagram

The memory, in broad lines, consists of the following parts (refer to fig. 12):

- Delay Line (4 parts)
It is used to time the various significant events in memory.
- Driving current adjustments circuits
They are used to determine the driving currents value.
- Driving generator (2 for reading and 2 for writing)
They are used to generate the currents in the selected position.
- Selection circuits (128 for 2 matrixes)
They serve to locate the memory position in which to perform a reading/writing operation.
- Inhibition generators (72 for 2 matrixes)
They serve for the writing logic.
- Reading amplifiers (72 for 2 matrixes)
They serve to detect the tension pulse from the sense wires coming out from the core planes and to bring the pulses themselves to standard logic levels.
- Strobe generator
It serves to operate a time discrimination between signal and noise coming out from the matrix sensewire.
- Matrixes
They consist of ferrite cores set on 9 planes, one of which serves for the odd parity check. Every matrix has 16384 positions (128 x 128) which can be detected along the two orthogonal axes X and Y.

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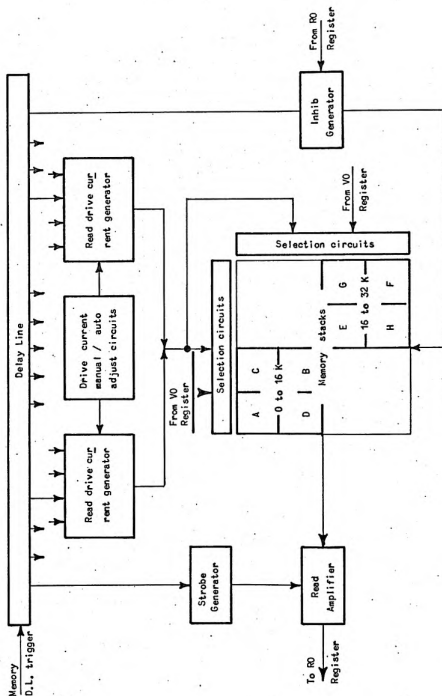


Fig. 12 - Memory Block schematic

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8.2.1. Delay Line

The sequence of events in memory is timed by pulses generated by a Delay Line.

The Delay Line consists physically of 4 parts (see fig. 13), 2 for reading (ch. 352 - 353) and 2 for writing (ch. 354 - 355).

The starting of the Delay Line occurs with the command VAMEA arriving from C.P.U.; this command is called MEMOA in memory.

A certain number of pulses with equal length (150 ns) are taken at different intervals from the Delay Line. All the pulses are taken from the Delay Line in fixed points with the exception of the MAO4 which requires a different positioning depending on the memory (refer to para. 8.2.6.2.).

Some pulses (ch. 370-5) are taken to supply the signal MEVA (valid memory) to the C.P.U.

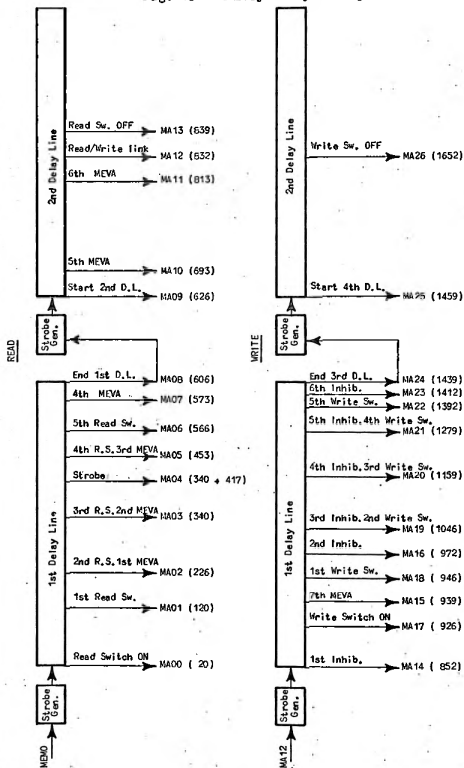
The cycle of this Delay Line is partially overlapped with the one of the C.P.U.

The period of the memory Delay Line is about 2 μ s.

In the average the memory access time is about 460 ns.

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Fig. 13 - Memory Delay Line portion



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MEMORY CYCLE

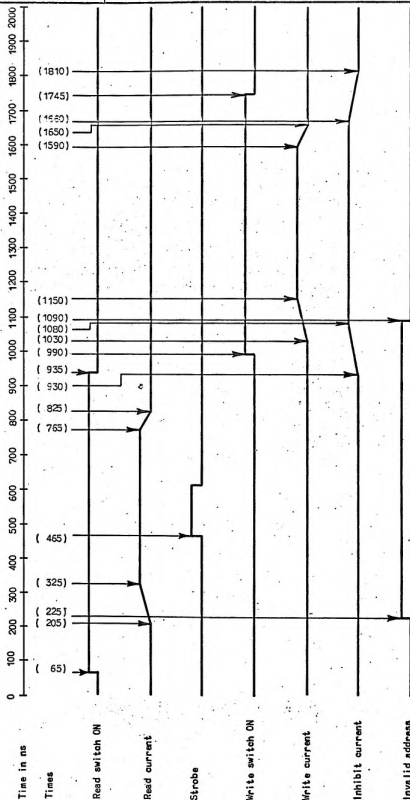


Fig. 14

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8.2.2. Driving currents adjustment circuit8.2.2.1. Reference voltage generator

This circuit serves to supply a reference voltage to the driving current generators (refer to fig. 15).

It consists of a power supply, stabilized at -20V which supplies a voltage of about -14V variable in function of the environment temperature (MERI signal).

The driving currents are proportional to the 6V voltage difference that there is between the signal MERI and the -20V; this voltage difference is independent from the -20V power supply voltage and is only in function of the environment temperature.

The sensitive element is a thermistor connected to a compensation resistive network having the characteristic to be able to vary its resistive value when the environment temperature varies.

The signal MERC serves for the memory margin evaluation circuit.

The driving currents vary of $\pm 7\%$ from 10 °C to 40 °C, having as reference a 6V voltage.

The circuit TERI and the thermistor assembly are physically located on the TEME2A board (ch.373-3).

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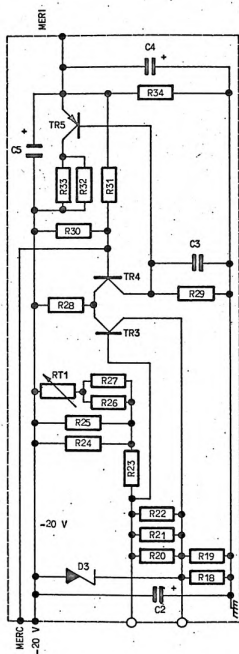


Fig. 15 - TERI circuit

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8.2.2.2. Memory margin evaluation circuit

This circuit allows to vary manually the reference voltage, signal MERI, and therefore the driving currents; physically it is located on the MAME board (ch. 350-1). On the MAME board there is a rotary switch DEVI with 6 positions for margin evaluation to which the following variations in percentage of the driving current I_p correspond:

Rotary switch position	I_p % variation
7	-8
8	-6
9	-4
0	0
1	+4
2	+6
3	+8

In the position "0", the driving current has the nominal value imposed by the TERI circuit of the TEME2A board therefore the function of the MAME board fails.

In the other positions, the MAME board acts on the TERI circuit inserting some additional resistances in the following way (refer to fig. 16):

- by inserting resistances between MERC and -20V, MERI increases;
- by inserting resistances between MERC and MERI, MERI decreases.

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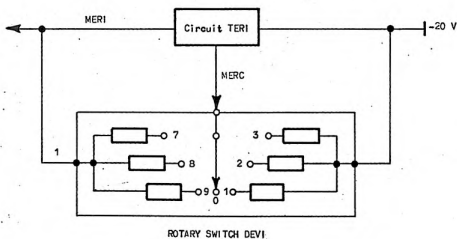


Fig. 16 - NAME circuit

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8.2.3. Driving generators

The reading and writing current generators used belong to the unidirectional type. .
For each ax, 2 current generators called PIME are used; in total 4 PIME are needed in the case both of one matrix only and two matrixes.

The 4 generators are used in the following way:

- 1 reading current generator, MOILI, for the ax Y (ch.370-9);
- 1 writing current generator, MOISI, for the ax Y (ch.371-9);
- 1 reading current generator, MVILI, for the ax X (ch.370-4);
- 1 writing current generator, MVISI, for the ax X (ch.371-4).

The generated current lasts for about 400 ns, its value is around 368 mA and its trailing edge is of about 115 ns. Every couple of reading or writing current generators is driven by an APIM circuit (ch. 370-3 and 371-3) at the inputs of which there are the reading or writing timing signals MILTA or MISTA and the reference voltage MERI.

The APIM circuit is physically located on the PIME board.

8.2.3.1. APIM circuit (refer to fig. 17)

The APIM circuit generates the wave form necessary to drive a couple of current generators.

The circuit is driven, through capacitive coupling, by two NANDs in cascade (ch. 371-1, 2 and ch. 370-1, 2). The first NAND uses 5 out of its 8 inputs to take from the Delay Line a number of pulses sufficient to supply the reading, MILTI, or writing, MISTI, timing signal to the APIM circuit.

The current raising time is determined by the capacities C4-C5 inserted on the TR3 transistor collector (fig. 17); Its width is instead established by the MERI reference voltage generated by the TERI circuit which acts as a cut ting voltage on the TR3 collector.

8.2.3.2. PIME circuit

The current generator consists of 2 transistors in parallel having a single output. The driving current is determined by the emitter resistances of the TR1 and TR2 transistors adjusted for this purpose (fig.18). The coupling with the memory wire was done through the T1 transformer which has a transformation ratio 1:1.

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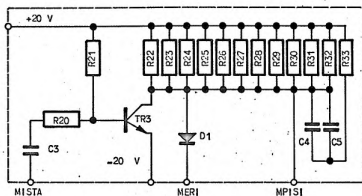


Fig. 17 - APIM circuit

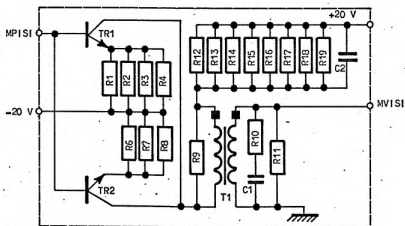


Fig. 18 - PIME circuit

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8.2.4. Selection circuits8.2.4.1. General

The memory consists of 1 or 2 matrixes with 16384 positions (128 x 128).

Every matrix is divided ideally in four quarters of 4096 positions (64 x 64) each identified by the letters A, B, C and D and E, F, G and H respectively for the 1st and 2nd matrix (fig. 19).

The two matrixes forming the memory are ideally set in diagonal (fig. 20). The selection of one of the two matrixes occurs with the FF V014 of the V0 addresser of C.P.U. (fig. 21)).

The particular order of selection of the quarters A, B, C and D for the 1st matrix and E, F, G and H for the 2nd matrix is obtained with the 4 possible combinations of the exclusive OR of the FF V012 and V013 (MEVO signal). The FF V013 has the task of selecting one of the two diagonals of each matrix, while the FF V012 selects the quarter within the diagonal itself.

Every matrix is divided in 8 groups, every one of which is driven by a switch called switch of group (INTE A).

Within every group each memory lead is chosen through 16 switches called switch of unit (INTE B).

The switches of the units, by groups of 4, are connected with some uncoupling circuits (REDI).

The direction of the driving current I_p in the memory circuits is the following: driving generator - uncoupling circuit - unit switch - matrix - group switch.

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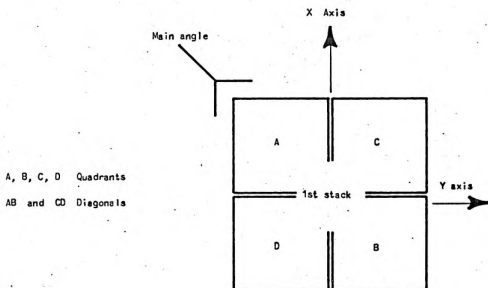


Fig. 19 - 1st stack

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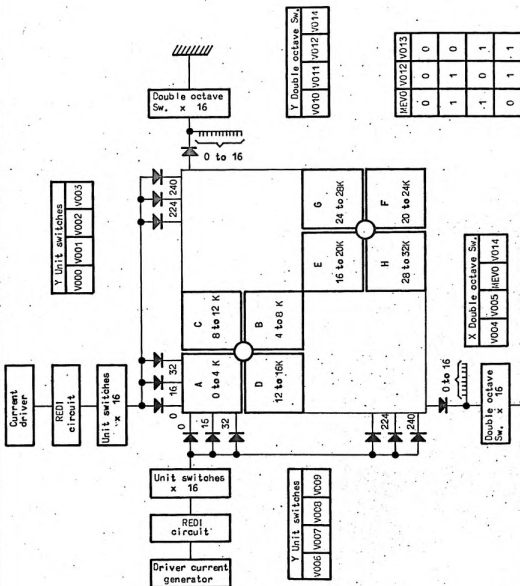
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Fig. 20 - Selection circuits and stack layout



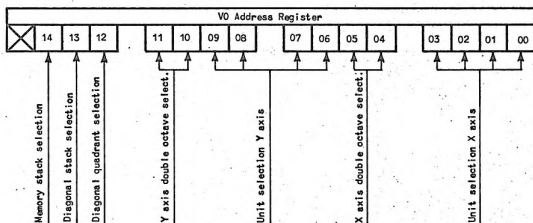


Fig. 21

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8.2.4.2. Organization of the selection logic

The memory module includes in the maximum version (32K) 128 interruption switches divided in 8 boards with 16 elementary switches each.

The types of switches used are two:

- Group switches on ground side (INTE A);
- Unit switches on ground generators side (INTE B).

For each ax, the switches are organized in two couples of sub-matrixes of 16 elements each (4 x 4): 1 couple for the group side and 1 couple for the unit side.

The switches of each sub-matrix are selected by the DRIV and SINC circuits (fig. 22).

The DRIV circuits of every couple of sub-matrixes are driven by 3 FF of the V0 addresser register of CPU, one of which serves to select the sub-matrix and two to select the DRIV circuits.

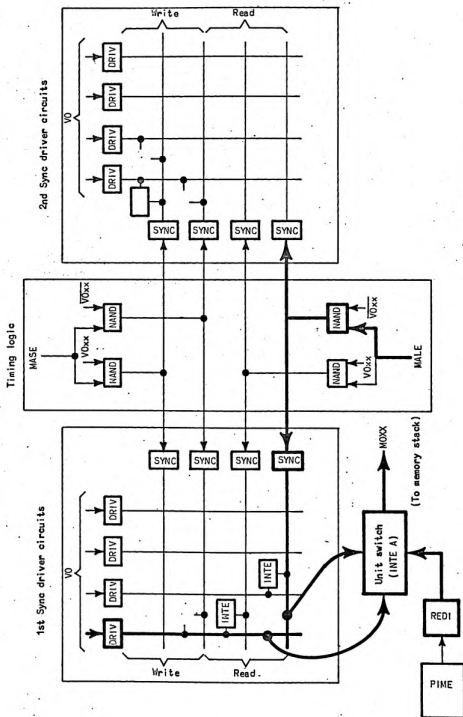
The timings (2 for reading and 2 for writing) arriving from the switches timing logic act on the circuits SINC of every couple of sub-matrixes.

The timings are common to the two sub-matrixes and are conditioned each one by a FF of the V0 register.

The use of the various FF of the register for the selection of the unit and group switches for the X and Y axes is the following:

	Selection			Name	
	Sub-matrix	DRIV	SINC		
UNIT - AX X	V003	V001 V002	V000	XX=00*15	XX=00*15
GROUP - AX X	V014	V004 V005	MEVI	XX=20*35	XX=20*35
UNIT - AX Y	V009	V007 V008	V006	XX=40*55	XX=40*55
GROUP - AX Y	V014	V010 V011	V012	XX=60*75	XX=60*75

Fig. 22 - One pair of sync driver circuits



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8.2.4.3. Switches timing

Such a circuit consists of two FF MALE and MASE (ch.360) used respectively to time the memory reading and writing phase.

The FF MALE and MASE are driven directly by the pulses generated by the Delay Line.

The circuit supplies the signal to time the reading MALn (n = 0-7) and the writing MASN (n = 0-7) used by the SINC circuit.

8.2.4.4. DRIV circuit (fig. 23)

The DRIV circuit consists of a TR1 transistor working from the switch and driven by a NAND at the inputs of which there are the FF of the V0 addresser register of CPU.

When the TR1 transistor is off, the 4 switches of the line of the sub-matrix connected to it are enabled to the performance.

8.2.4.5. SINC circuit (fig. 24)

The SINC circuit consists of a TR2 transistor driven by a NAND at the inputs of which there are the MALn or MASN timing signals.

When TR2 is on it enables to the performance one of the 4 switches of the column of the sub-matrix connected to it.

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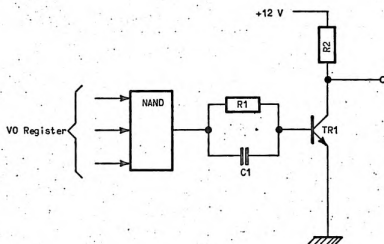


Fig. 23 - DRIV circuit

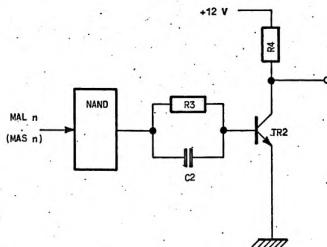


Fig. 24 - SINC circuit

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8.2.4.6. REDI circuit (fig. 25)

The REDI circuit has the task to uncouple, by group of 4, the switches of the reading or writing units from their respective driving current generators; the degrading of the trailing edge of the driving current I_p due to parasitic capacities is thus avoided.

The REDI circuit consists of a D1 diode placed in the sense of the current and polarized by a R1 resistor referred to +20.

8.2.4.7. Group switch (INTE A) (fig. 26)

It serves for the selection of the memory leads on ground side; it consists of a TR1 transistor driven by the secondary wiring of a T1 transformer.

The TR1 emitter is connected to ground while the collector is connected to the divider diodes with 16 subsequent memory leads (e.g.: leads 0 - 15).

8.2.4.8. Unit switch (INTE B) (fig. 27)

It has the task to select the memory leads from the driving generator side; it consists of a TR2 transistor driven by the secondary wiring of a T2 transformer.

The TR2 collector is connected to the driving generator through an uncoupling circuit REDI, the emitter is connected through the divider diodes with 16 memory leads with an interval of 16 between each group (e.g. 0-16-32-48 . . . 208-224-240).

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8.2.5. Inhibition circuits8.2.5.1. General

The memory module has, in the maximum version (32K) 72 inhibition generators divided in 9 boards with 8 elementary circuits in each.

Every board contains the elementary circuits related to two subsequent plans of the matrix, with the exception of one which contains the ones concerning plane "0" of both matrixes.

The organization of the inhibition logic divides the 9 planes in even and odd planes.

Each plane of the two matrixes is divided in 4 inhibition windings (8 for the 2 matrixes).

Every winding covers a zone of 4096 cores (128 x 32) called Strip.

The strips of the even planes are set perpendicularly to the ones of the odd planes (fig. 28).

The selection of one of the 8 strips (0+3 for the 1st matrix, 4+7 for the 2nd matrix) of the even or odd planes is done using the VO addresser of CPU and precisely:

- even planes strips FF V005 - MEVO - V014

- odd planes strips FF V011 - V012 - V014.

8.2.5.2. Inhibition logic timing

The timing signal of the inhibition logic MAGI (ch.371-5) is obtained making the OR of 6 pulses generated by the Delay Line.

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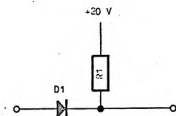


Fig. 25 - RED circuit

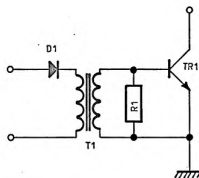


Fig. 26 - Double octave switch (INTE A)

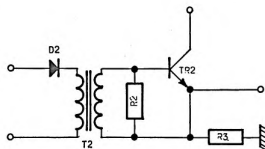


Fig. 27 - Unit switch (INTE B)

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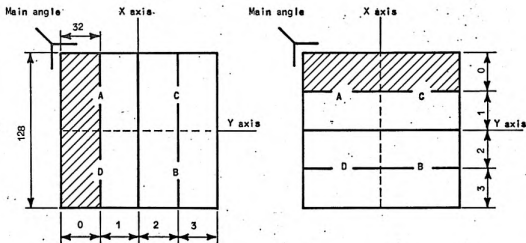


Fig. 28 - Even (right) and odd (left) inhibit strips for 1st stack

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8.2.5.3. Selection of strips and planes (fig. 31)

The signal MAGI conditioned by the interested FF of V0 supplies the timed commands MTPm and MTDm ($m = 0 \div 7$: strip indicator).

These signals are used to select one of the 8 strips (4 for each matrix) respectively of the even and odd planes (refer to ch. 390 - 391).

The choice of the plane is obtained conditioning the timed commands with the signals MNOn ($n = 0-2-4-6-8$ for the even planes and $n = 1-3-5-7$ for the odd planes).

The signals MNOn arrive from register R0 of the CPU with the names ROOn ($n = 0-7$), ROO8; and they change names passing through the strappings on the NAME board (refer to ch. 350).

The obtained signal is called LBnm (n = plane indicator, m = strip indicator).

8.2.5.4. Power circuit (INIB - Fig. 30)

The power circuit is driven by two NAND's in parallel driven by the LBnm signal.

The coupling between the matrix inhibition lead and the related power circuit is obtained through a T1 transformer. The inhibition current circulating in the secondary circuit is obtained making the transistor TR1 whose collector is connected to the primary winding of T1 work as a switch (the other terminal of the primary winding of T1 is connected with the REIN circuit).

The transformation ratio is 1:1.

8.2.5.5. Adjustment circuit (REIN circuit - refer to Fig. 29)

9 elementary circuits are assembled on every REIN board. Every circuit consists of a RC group; a terminal of the group is connected to the collector of the TR1 transistor of the power circuit through the primary winding of T1, while the other terminal is connected to the +20V voltage. The resistance determines the value of the inhibition current (about 340 mA), the capacitor the period of the trailing edge of the current itself.

Every REIN circuit drives the 8 power circuits related to the same plane of the two matrixes. A suitable timing (MTPm or MTDm) allow to enable every circuit individually.

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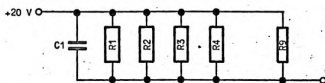


Fig. 29 - REIN circuit

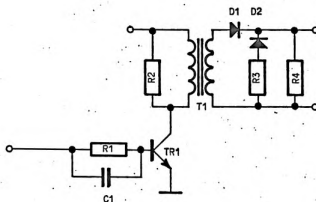


Fig. 30 - INIB circuit

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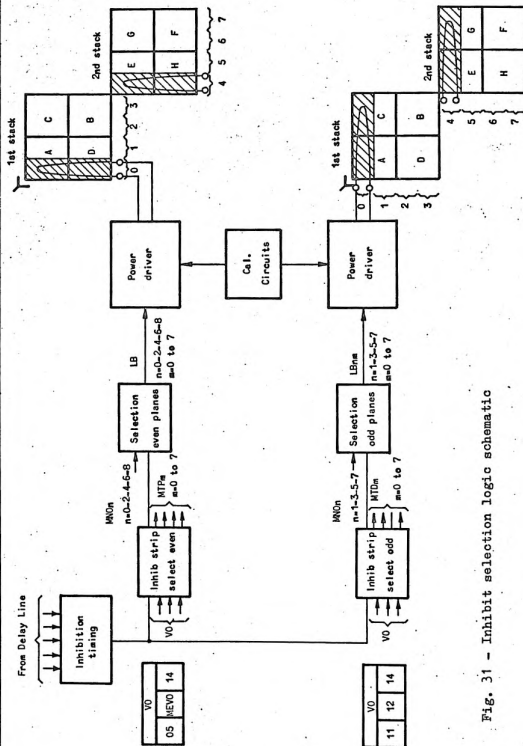


Fig. 31 - Inhibit selection logic schematic

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8.2.6. Read circuits8.2.6.1. General

The memory module has in the maximum version (32K) 72 read amplifiers divided in 8 boards with 9 elementary circuits each.

Every matrix plane is divided in two diagonals of 8K formed by the quarters AB-CD for the 1st matrix, EF-GH for the 2nd matrix.

In every diagonal, there are two sense wires which are connected to amplifiers.

Every sense wire includes in every quarter half of the cores; the sense wires are wired with such a geometry in order to obtain a high signal-noise ratio.

The signals obtained by the commuting of the selected core in case of "1" reading, have a width of about 40 mV and may show at the terminals of the sense wire with positive or negative polarity.

In order to obtain a conversion of the signals at logic levels, we perform:

- a width discrimination
- an amplification
- a time discrimination.

8.2.6.2. Width discrimination

The width discrimination on the signals coming out from the sense wire is obtained through a double resistors network (RETED circuit) supplied by the signal META (+12V). This voltage serves to create a 20 mV fixed threshold so that signals below this value are not considered as "1".

8.2.6.3. Differential amplifier

The differential amplifier consists of integrated circuits and has two equal sections with a single output. It has the task to amplify all the signals collected by the sense wire, above the input network threshold. Depending on whether the signal taken from the sense wire is positive or negative, one section or the other will be working.

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The 1 and 2 strobe inputs on the differential amplifier are in parallel and they are used for the time discrimination.

The LEAnp or LEBnp signal (n = plane indicator; p = sense wire indicator) obtained at the output is the result of the AND between the strobe and the amplified signal.

8.2.6.4. Time discrimination

The time discrimination is obtained through the strobe circuits.

The strobe signal is obtained with the MA04 pulse of the Delay Line which determines also its length (ch.370-371). The strobe circuits and their improvements are physically located on the PIME2A board.

Each one of the 4 MASTx strobe signals (x = 1 - 4) supplies all the amplifiers of a diagonal.

NOTE: In order to make an exact discrimination of the signal coming out from the differential amplifier it is necessary to maintain constant the time elapsing between the trailing edge of the read driving current (analogic stages) and the strobe (logic stages).

In order to obtain this result it is necessary to position the output of the MA04 pulse (strobe timer) with respect to the MA01 pulse (1st pulse of read PIME timing) every time that the read PIME board is replaced.

Initials printed on the PIME in Q16	A	B	C	D	E	F	G	H	L	M	N
Kstrapping position on Delay Line in Q15	O7 N7	O6 N5	O5 N5	O4 N3	O3 N3	O2 N3	O1 N3	R2 N3	R3 N3	R4 N3	R5 N5

8.2.6.5. Wired OR and logic OR (fig. 35)

The wired OR consists of the physical connection of the outputs of the amplifiers of diagonals AB - EF and CD - GH of each plane.

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The logic OR is obtained through the AMOR circuit of the LOGI2C board (ch.388) which performs the logic OR of the two diagonals above mentioned.
The resulting signal LEO_n (n = 0 - 8 plane indicator) is sent to the CPU R0 register.

8.2.6.6. -6V generator (fig. 34)

This circuit supplies the -6V voltage used by the differential amplifier.

The circuit consists of 2 transistors TR1-TR2 connected to an emitter-follower whose bases are supplied with constant voltages through 2 zener D1 and D2.

The resistance between the emitters and the parallel of the two zeners serves to increase the reliability degree of the circuit as the output voltage must not be above 7V.

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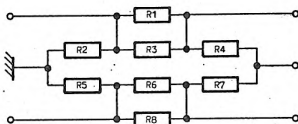


Fig. 32 - RETED circuit

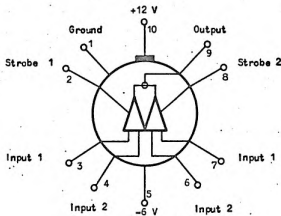


Fig. 33 - Read amplifier

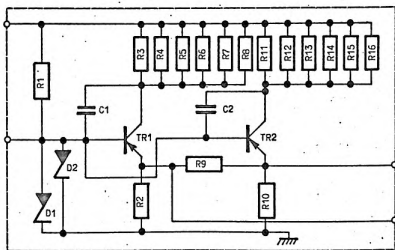


Fig. 34 - -6 V generator

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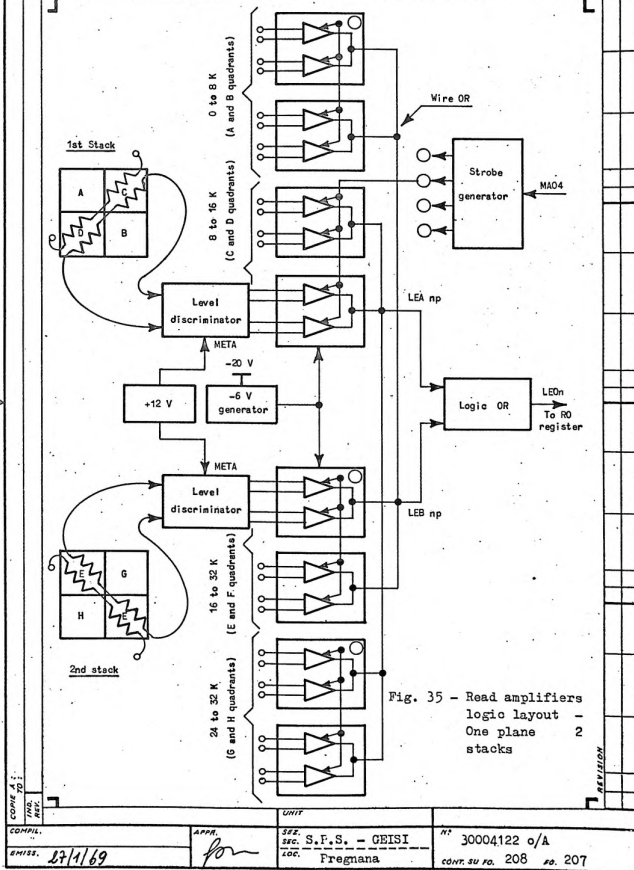


Fig. 35 - Read amplifiers
logic layout -
One plane 2
stacks

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8.3. Memory composition

The memory (1 module) of the GE 130 is interconnected to the Central Processor.

This assembly and the circuits common to all versions form a single elementary unit: UCE 460.

The matrixes and the boards additions necessary to obtain the various memories capacities form other elementary units.

The composition in elementary units of the Central Processor in function of the different memory capacities is the following:

Versions	Elementary units
8K	UCE460 + 1 MEM470
12K	UCE460 + UCE461 + 1 MEM470
16K	UCE460 + UCE462 + 1 MEM470
24K	UCE460 + UCE463 + 2 MEM470
32K	UCE460 + UCE464 + 2 MEM470

in which:

- UCE460: Central Unit (4 $\frac{1}{2}$ modules not differentiated as far as the memory extension is concerned).
- UCE461: boards addition to pass from 8192 to 12288 memory positions.
- UCE462: boards addition to pass from 8192 to 16384 memory positions.
- UCE463: boards addition to pass from 8192 to 24576 memory positions.
- UCE464: boards addition to pass from 8192 to 32768 memory positions.
- MEM470: 1 memory matrix

8.4. Matrix description

The matrix (MEM470) consists of the following parts (drawing No. 14053098):

- 9 planes (with 16384 cores) one besides the other;
- 1 driving wire for every column of the ax X;

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- 1 driving wire for every row of the ax Y;
- 4 inhibition wires for every matrix plane;
- 4 sense wires for every matrix plane;
- 4 boards of separator diodes (2 DIRE A and 2 DIRE B).

The introduction of several sense and inhibition wires and the special geometry with which they have been wired has allowed to reduce considerably the noises.

8.4.1.

Driving wires

The matrix driving wires are connected with the selection logic of the memory through the boards DIRE A and DIRE B containing the separator diodes and the resistances to refer to +12.

These boards are set externally to the cores planes. The inputs of the read driving wires (outputs for write) are on plane "0" for the ax X and on plane "8" for the ax Y.

The read outputs (inputs for write) are on plane "8" for the ax X and on plane "0" for the ax Y.

The denominations X0, X1, . . . Y0, Y1 . . . indicate current read inputs (write outputs) while the denominations X0', X1', . . . Y0', Y1' . . . indicate the current read outputs (write inputs) (refer to fig. 36).

The functions of the separator diodes and of the resistances referring to +12V (refer to fig. 37) are those of uncoupling dynamically all the lines driven by the same switch thus avoiding that the capacitive currents flow in the unselected memory lines.

The physical location of the diodes and of the resistances and their interconnections with the matrix may be seen on the logic diagrams of the MEM470 (ch. 500 - 511).

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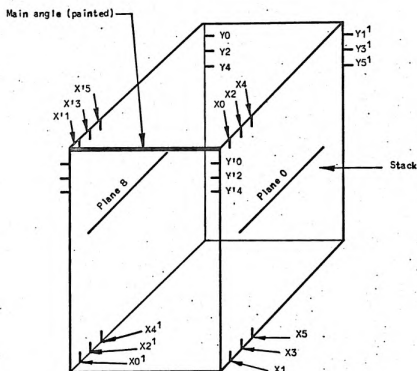


Fig. 36 - Stack

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8.4.2.

Sense and inhibition wires

The matrix sense and inhibition wires are connected with the memory logic through connectors J1 and J2.

The connection between the matrix and the above mentioned connectors is done with a TWIST wire.

The input and output terminals of the inhibition and sense wires physically are located as indicated on drawings No. 14003082 - 14003083 of the MEM470.

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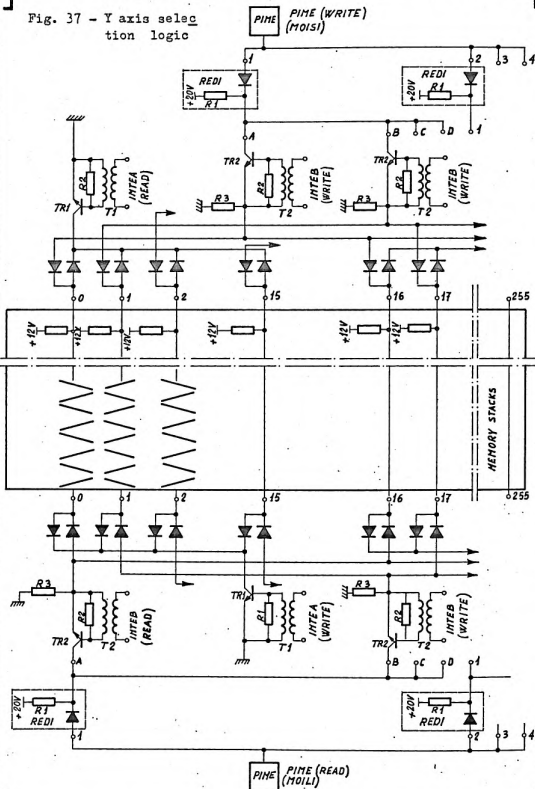
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Fig. 37 - Y axis selection logic



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9. DETAILED DESCRIPTION OF THE C.P.U. COMMAND LOGIC9.1. General

The external instruction calls, as we have already seen, for a memory sub-field.

The characters of this sub-field supply the additional information required to perform the external instruction. These characters are read and interpreted after the α phase.

This second phase is called phase to organize the external instructions or general β phase.

In the case of SPER, LPER, EPER, CPER, the instruction ends after the performance of this phase.

In the case of TPER, at the end of the general β phase the real data transfer starts.

The general β phase is performed also in the case that the program loading is to be performed, i.e. the introduction in memory from the address 0/0 0/0 onward of the program which will be performed afterwards.

During this phase, characterized by the FF AINI position ed in set with the switching of the "LOAD" key from the operating panel, some commands are inhibited that would normally be issued, and others specifically connected with program loading will be issued.

In the case the external instruction uses a transmission channel or a C.P.U. connector already busy with another transfer instruction, an automatic waiting re-cycle occurs consisting of:

- positioning the program addresser on the function code of the peripheral instruction (decounting 4 positions);
- going back to the beginning of phase α re-examining the peripheral instruction not performed and so on, until the selected connector and channel are free.

This re-cycle is necessary in order to be in condition to detect and, if necessary, to fulfill any possible interruption requests, thing that occurs during phase α . The automatic re-cycle occurs also considering the selected peripheral unit status only if the instruction must be performed with a waiting for the unit free. The only instruction which is not blocked by the busy channel or connector condition is LPER which has the task to examine the busy channel and connector conditions and to generate as a consequence the qualitative result.

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9.2. Sequence of general β phase

The general β phase is reached after having performed phase α and with the machine devices set in the following way:

- P0 contains the address of the function code of the instruction subsequent to the peripheral one;
- F0 contains the configuration 9/E in the case of PER and 9/C in the case of PERI;
- L1₂₁ contains the character "C" (containing the unit name: U in case of PER).
In case of PERI this character is not used;
- V1 and V2 contain the address of the 1st character to the left of the sub-field.
To scan the sub-field the register V2 is used.

The sequence of the states performed during the general β phase differs substantially on the type of PER performed.

Using the Flow-charts (14023130 fig. 13 and 14) analyze the different operations performed.

- Status 65/64

If the instruction is a PERI, the character C which was stored in L1₂₁ during the phase α , is replaced with the content of the 224th memory position.

- Status C8

The character Z, first character of the sub-field, is read from memory and it is stored in L2. During program loading L2 is cleared, blocking memory reading (one is forced Z=0/0).

If the channel or the connector selected are busy F105 is set and then a decount is done in P0, if necessary.

F104 is reset to enable, if necessary, a 8 μ s waiting period between the issue of AEBE and the return of the peripheral unit conditions.

- Status D8

If the channel and the connector are free, the "Enable channel selection" command is issued (this permits the issue of the peripheral unit strobe, AEBE) Character U,

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that represents the unit name, is loaded in register RE to be then forwarded to the interface.

If to the contrary, PO counts -1.

The reason for the decount is, for the machine, to position itself on the function code of the pertinent peripheral instruction, after the following stati have been done, so that it can re-enter the instruction to then complete it. This recycle finishes when both the channel and the connector are free.

No recycle is done if the instruction is a LPER for channel or connector busy.

- Status D9 and DA

These two stati do two further decounts on the program addresser PO (if necessary) in the same way described as for Status D8.

- Status D8

Does a 4th decount on PO (if necessary) and sets FIO4 which was put in reset during Status C8.

Two ways are open after Status DE.

- 1) If both the channel and the connector are free (FA05), as FIO4 is copied in FA04 only at the beginning of the next Status, a recycle is done on Stati D8, D9, DA and DB which will not carry out any meaningful operation.

This recycle is done only once because FA04 will be in set at the next passage.

The reason a recycle is performed is to introduce a gap between the issue of the unit selection signal AEEB (Status D8) and the instant in which the interface conditions on the unit itself are scrutinized. This gap is to give settling-down time to the logic levels present on the selected unit interfaces.

- 2) If either the channel or the connector are occupied, and thus PO is holding the configuration of the function code of the peripheral instruction, the program enters Status DC.

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- Status DC
 - V3 is transferred in V1. This operation is done for a SPER instruction to unload in V1 the final address of the transfer using channel 3.
 - RO takes on the 0/1 configuration, which corresponds to the exam configuration for the unit free condition. If the unit is not free (PCOV) and if the instruction envisages to wait for unit free (L202, L2 contains the Z) and if switch SITE is released, (AITE), FIOO sets to enable the forthcoming wait recycle.
 - If the instruction is inherent to channel 2 (L200) and if both the channel and connector are free (FA05), the timer SI is loaded with the 1st configuration of the data exchange sequence inherent to channel 2.
- Status CC
 - If program is not in the initial program loading phase, the subfield character X is read from memory and is loaded in RE. If there is no data exchange under way on channel 3 (FUC3), character X is also stored in RA.
 - Configuration 4/0, representing the read forward command, is loaded in RE during initial loading.
 - If FIOO had been previously set (Unit busy), FIO5 sets to enable the wait recycle after having decounted in PO during statuses D8, D9, DA and DB.
 - If the instruction is an EPER or an LPER, FIO5 sets if necessary. FF FIO5 is now considered as the qualitative flip-flop to store the condition occurred signal.

The sequence, from Status CC, can follow 4 different ways:

- 1) With FA05. FA00 the sequence reaches back into Status D8 to do a decount in PO. This is necessary to carry out a wait recycle for unit free.
- 2) A return to phase α is done if the unit is busy and if condition FA05 is present the second time that Status CC is entered into. For an LPER the instruction is considered finished, thus the sequence returns to phase α .

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- 3) If the instruction is a SPER (FA00.FA05.DU96.DU95), the sequence goes to Statuses EA and EB, which perform the unloading of channel 3 conditions.
- 4) If the instruction is either a CPER or a TPER and all the conditions set down necessary to continue the sequence have been satisfied, Status CA is entered.

- Status CA

The I/O (CE03) command is always issued. This command resets particular channel logic conditions. Furthermore, only in the case that the instruction is a CPER (L207), the following operations are carried out:

- Signals VICU and TU2I1 accompanying the command whose configuration has either been loaded in RE or in RA during Status CC are sent to the interface.

- If the selected connector is either connector 3 or 4 (LI07) or is connector 1, operating in unison with channel 1 (MB Standard Printer - LI06.L200), the execution of the operative cycles ceases waiting for the command receipt (TE30) through the command reset signal RIAP.

In this case, until the command receipt is delivered, the machine does some statuses O/O (display) because these are no cycle requests (when operation is not in overlap).

Status CA is the last meaningful Status that is performed for a CPER instruction before the α phase of the following instruction.

If a TPER is considered, the sequence goes to Status A8.

- Status A8

If the program is not being initially loaded (AINI), the first byte representing the length is read - off from memory and loaded in L143.

During initial loading, L143 is zeroed.

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- Status A9

AINI enables the reading from memory of the second byte expressing the length and memorizes it in L121. If the instruction belongs to channel 3, the contents are transferred into register L3.

During initial program loading register L121 is preset with configuration 8/0 which corresponds to a length of 129 characters.

- Status AA

AINI enables the reading from memory of the most significant byte of the address and transfers it in V143. During initial loading, V143 is zeroed.

- Status AB

If the integrated parallel printer (I.P.P.) (PC11.PC21) is not interested by the instruction, AINI enables the reading from memory of the least significant byte of the address transferring it in V121.

If instead the instruction does interest the I.P.P., V121 is zeroed.

The contents of V1 are loaded in V3 if the instruction is on channel 3.

If channel 2 is used, V1 is put in V4.

During this Status, the I/O command (CEO1) is issued to enable the set condition of the following flip-flops:

- 1 - RASI, PUC2 and PUC3. These identify the transmission phase for channels 1, 2 and 3 respectively.
- 2 - PEC4. Has the purpose of removing the selection on channel 1, with which the instruction on channel 3 was initiated, when the data output transfer phase starts on channel 3.
- 3 - RUSC and RIND. These memorize the mode of transfer pertaining to channel 3.

Flip-flop VICU sets and the command accompanying TU201 is issued.

If neither the reader nor the integrated printer are interested (PC12 + PC11 + PC21), the command to enable the reset of RIAP is issued in waiting for the command received.

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If the "enable reset of RIAP" is issued and the sequence is not in overlap, the machine does O/O cycles up to the arrival of the command receipt. It then passes to Status B8.

- Status B8

If it is the first time that Status B8 is being done (FA00), if the sense of transfer is in input (L206) and if the command has been accepted (RAC1), a character request TU101 is emitted.

The arrival of a TU101 at an integrated card reader, causes the feeding of one card.

If the instruction is a preparatory instruction for channel 2 (L200.L203), flip-flop F102 sets which, if the instruction straight following the present one is a TFER on channel 1, sets the overlap of data transfer on channel 1 and 2, with mode 115.

After Status B8 has been completed, the Processor behaves in different ways depending on the channel used and on the eventual other transfers under way using overlap.

- 1) - If the transfer is inherent to channel 3, condition DU98 is verified. This causes Stati EA and EB to be done which unload on the qualitative FFs: any information belonging to a refused command (RAC1), and phase α is again entered into. The selection of channel 3 is removed, for a refused command, through special command CE19. If the operation is already under way, Stati EA and EB are done with the consequent re-entry in the α phase. Data transfer phase is done in overlap with the other program instructions, in the following way:
 - when a work cycle is assigned to channel 3, signal RES3 forces one in NAOO, whose contents are then transferred in SAOO.
 - The logic sequence matrix does a state O/1 which is, in fact, an I/O transmission Status relative to channel 3.
 - With no requests present, internal calculations are performed.

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- 2) - If the transfer is relative to channel 2, two conditions are present:

- The instruction is in overlap.

In this case, through condition DU97 a re-entry in phase α is done and the data transfer is done in overlap.

Each time a channel 2 request arrives, signal RES2 drives the logic sequence matrix with the configuration drawn from the SI sequencer.

- The instruction is not in overlap.

The condition DU97 only occurs at the end of the transfer on channel 2 (PUC2).

During those cycles in which there are no channel 2 or channel 3 requests, Stati B8 (non-operative) are carried out.

- 3) - If the instruction is relative to channel 1, the following two conditions are pertinent :

a) - The command has been refused (RAC1)

- If the instruction has been preceded by an instruction on channel 2 in overlap, it is necessary to wait for the end of the instruction on channel 2 to check the DU98 condition (PC01 PUC2.RAC1) and go to Stati EA and EB which reset the end-of-transfer conditions.

In the mean while, the Processor carries out, in the cycles not used by channel 2 or 3, some non operative B8 Statuses through the SO sequencer.

- If the instruction was not preceded by an instruction on channel 2, Statuses EA and EB (PC01.PAC2.RAC1) are done immediately with a re-entry into the α phase.

b) - The command has been accepted.

If the command has been accepted, the transmission phase starts.

As long as there are no channel 1 data exchange requests, the Logic Sequence Matrix carries out:

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- Some waiting B8 Statuses, through S0, if no channel 2 or channel 3 requests are present.
- Some Statuses 01 when channel 3 requests are received.
- Some channel 2 Statuses, through SI, when channel 2 requests are present and during the absence of channel 3 requests.

As soon as a channel 1 request is received, S0 (B8) is copied in NA. Furthermore, RESI forces ones in NAOO.

Therefore the Status done is B8+1=B9, which is the Status dealing with channel 1 data exchange.

9.3. Input data exchange sequence with packing on channel 1.

If the exchange of input data has to be done in packed mode (L204=0), the Statuses done for each request are B9 and B1.

For this reason, the command to enable the reset of RIAP is inhibited with L204 during Status B9, for which reason Status 1 is immediately entered.

During Status B1 the reset of RIAP is enabled and a wait is done for the next character accompanying the trigger. See Flow Chart 14023130, Sheet 15.

9.4. End of operations on channel 1

9.4.1. End from CPU

The end from CPU condition occurs in the following cases:

- RILAA (141-1) = 0, when:
 - L1 contains all zeroes and the transmission is with normal characters (L1ZE6.L2046).
 - L1 contains all ones and the transmission is with packed characters (RLIU1.FA016).
- PAZ1A (141-6) = 0, when:
 - Signal PEZ1A is present (enable disconnect from DATA-NET) and an instruction on channel 2 has finished (PUC26=0).

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These conditions generate signal RILE1=1 (141-2).
 RILE1 sets flip-flop RILI1 with end from CPU meaning.
 RILIA (138-9) goes to "0"
 RIVE1 (138-10) goes to "1"
 RIVEF (138-11) goes to "0"

a) For input transmissions

Signal RIF3A (139-11)=0 becomes active and sets REN21 (139-7).

REN21 issues signal TU201 to set RUF1 which, in turn, provides to the removal of the selection on channel 1 and to the issue of signal FINU to the interface.

b) For output transmissions

RIVI1 (138-18) generates REMAA at "0" (138-19) at the arrival of the TE30 (RB111) with RES11=0 and sets flip-flop RENI1 (138-20).

Flip-flop RENI1 sets REN21 through signal RIF4A (139-16).

With REN21 at "1", signals FINU and TU20 are generated as per the case of input transmission.

9.4.2.

Terminate from Peripheral

The condition of Terminate from Peripheral (RP101) is stored in flip-flop RIG11 (138-5).

This loading occurs in the following manner:

- At the arrival of a TE30 (RB111) for output (RTUE1) with RES11=0.
- At the issue of a TE30 (CE111) for input.

Two cases occur after this:

1) Output

RIG1A (138-3) = 0
 RIVEF (138-11) = 0
 REMAA (138-19) = 0 sets
 RENI1 (138-20)
 RIF4A (139-6) = 0 sets
 REN22 (139-16)

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REN22 sets RUF12 (139-20), with the T065 of the following cycle, which issues signal FINU.

REN21 also issues RT121 (139-14) which generates the TU20 accompanying signal FINU.

2) Input

RIG1A (138-3) = 0

RIVE1 (138-10) = 1

RIF3A (139-11) = 0 sets REN22 (139-16)

REN22, at the T065 of the following cycle, sets RUF12 (139-20) which issues signal FINU and removes the selection from channel 1.

REN21 also issues RT121 (139-14) which generates the TU20 accompanying signal FINU.

At the end of the transfer, if the Processor is working in overlap on channel 2, the end of transmission on channel 2 is awaited for, before going to Statuses EA and EB (RAS1 . PUC2.PC01). If there is no operation in overlap, on channel 2, the sequence goes immediately to Statuses EA and EB (PUC1.FA02.RAS1).

9.5.

Disparity error on channel 1

Flip-flop RERI (139-2) stores the disparity check error inherent to input data on channel 1.

Flip-flop RERI can also be set for disparity error on channel 3 during the unfolding of a SPER instruction.

The flip-flop-set conditions pertaining to data exchange on channel 1 are:

a) RES16=1

When the cycle has been given to channel 1.

b) PEST1=1

When the check network finds a disparity error and the "enable set external error" command (141-15) is issued.

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c) TO70=timing.

The 2nd set path is given by signal R31K1=1 (139-3) which is equal to RER32.CEO61 (141-15).

RER32 is the storing flip-flop for error on channel 3 for input data.

CEO6 is the command that enables the set for error 1 issued during Status EB of the general β phase for a SPER instruction. It is either reset by signal REFEA=0 (138-8) and driven by signal CAGU7=1 or during Status CA of the general β phase of an instruction pertaining to channel 1.

9.6. End of operation on channel 39.6.1. Terminate from CPU

When L3 contains all zeroes, RL301 at 1 (146-12) sets flip-flop RIL31 (146-13). This has the meaning of Terminate from CPU.

RIL3A (146-9) goes to 0

RIVA1 (146-10) goes to 1

RIVAF (146-11) goes to 0

- For input transmissions, signal RIF1A=0 (147-11) which sets RAN21 (147-7) is checked.
RAN21 issues a TU20 and sets RUF31 (147-18) which removes the selection from channel 3 and causes the forwarding of signal FINU towards the interface.
- For output transmissions, PTV31 (146-18), at the arrival of the TE30 (RB311) and with RES31=0, generates RAMAA (146-19)=0 and sets flip-flop RANI1 (146-30). Flip-flop RANI1 sets RAN21 (147-7) by means of signal RIF2A (147-6). RAN21 issues FINU and TU20 as seen for output transmissions.

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9.6.2.

Terminate from Peripheral

The condition of terminate from peripheral unit (RF301 , 146-3) is stored in flip-flop RIG 31 (146-5).

The condition is stored in the following way:

- In output (RTUA1=1) at the arrival of the TE30 (RB311) with RES31=0.
- In input, at the issue of the TU30 (CE141).

This occurs in two cases:

- In output : RIG3A (146-3)=0
RIVAF (146-11)=0
RAMAA (146-19)=0 sets
RANI1 (146-20)
RIF2A (147-6)=0 sets
RAN22 (147-16)

Flip-flop RUF31 (147-18) is set by RAN22 at the TO65 of the next cycle. RUF31 issues FINU.

RAN21 also issues signal RT321 (147-14) which, in turn , issues the TU20 accompanying signal FINU.

- In input : RIG3A (146-3)=0
RIVA1 (146-10)=1
RIF1A (147-11)=0 sets RAN22 (147-16)

RAN22, at the TO65 of the next cycle sets RUF31 (147-18) which issues signal FINU and removes the selection on channel 3.

RAN21 also issues signal RT321 (147-14) which issues the TU20 accompanying signal FINU.

As the selection is removed from channel 3, data transfer in overlap mode, on channel 3, comes to an end.

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9.7. Disparity error on channel 3

The disparity error condition on input data on channel 3 is stored in flip-flop RER3 (147-2).

Set conditions are the following:

- RES36=1. Cycle attributed to channel 3
- PEST1=1. Check error found and conditioned to the set of external error.
- TO702= Timing.

Flip-flop RER3 is reset either through signal REFAA = 0 (146-8), issued by signal CAGU7=1 or during Status CA of the general β phase of an instruction belonging to channel 3.

9.8. Sequence on channel 2

The 4 bit sequencer SI register is used during data exchange on channel 2.

The configuration 1100 (C) is loaded in SI during Status DC of the general β phase.

9.8.1. Channel 2 linked to connector 2 (CR)

At every cycle attributed to channel 2, Status OC is carried out. During this Status, the following operations are done:

- 1 - Data coming from the peripheral unit are written in the memory address given by the configuration contained in V4.
- 2 - The address configuration of V4 is updated by counting +1 for integrated card reader and -1 for magnetic reader.
- 3 - A reset if RIAP is enabled and a wait is initiated to wait for the next trigger from the reader.

Other operations are not meaningful.

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End of Transmission conditions reset flip-flop PUC2 which, together with the conditions mentioned above, causes the branch out from the transmission phase.
Herefollowing are given the possible conditions that can cause end of transmission.

9.8.2.

Terminate from reader

- FELEA=0 (LUF01.LU081) (125-15)

This signal is generated if the reader goes out of service.

- PF22A=0 (FINI2.PC221) (161-14)

Signal FINI is generated by the reader with the issue of the last trigger LU08.

9.8.3.

Terminate from CPU

- REFO5A=0 (VO216.PELM6) (149-3)

When a magnetic reader is used, the terminate is issued when the decoding of the least significant part of the VO addresser is equal to 2.

- RFO6A=0 (VOZ26.PELS1.POMO2) (149-7)

Terminate from CPU occurs, for a reader in normal mode, with the decoding of the 81st scanned memory position.

- RFO4A=0 (FELS1.VOZ36) (143-3)


In the case of a normal reader in normal reader mode, the terminate occurs with the decoding of 161st scanned memory position. 3

9.8.4.

Channel 2 linked to connector 1 (Integ. Printer)

For clearness sake, operation in non-overlap mode will be described.

After having initiated a TPER for MZ and having done Status B8 and at the arrival of the photodisc codes, signal PA21A=0 (133-4) is obtained which sets flip-flop REAB (143-14).

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Signal RUGO1 (143-12) is at "1" (RICI1=0), therefore RIMZ4 (143-13) going to zero satisfies the requests for the cycles on channel 2.

After this, Status O/C is then performed, during which the photodisc code contained in the NE network is stored both in the register RI and in first memory position used of the printed row.

The enable of RIAP has no effect on RIMZA, for which reason Status O4/O6 is done next.

The first time O4/O6 is done with the O/4 configuration. The operations done are:

- 1) Writing of the photodisc codes also in the 2nd memory position of the printed row.

NOTE: The first and second memory positions are used to determine the end of print.

- 2) Count +1 in V4.
- 3) Other commands issued have no effect.

The next Status done is O2/O3, in which the following operations are performed:

- a) - The first significant position of the printed row is read.
- b) - A +1 count is done in V4.
- c) - The datum read is compared with the photodisc code held in RI through the Arithmetic Unit. For equality, the AU gives decoding UAZO=1. This comparison is stored in flip-flop RINO (144-21). Flip-flops RINO and RINI make up a shift register to store the results of the comparisons between memory and photodisc so to condition the issue of the TUO2s enabling the chosen printing hammers.
- d) - Command CE16 is issued to load the buffer made up of flip-flops RICO and RICI (142-6-18). The purpose of RICO and RICI is to store the fact that one memory position has been read.

NOTE: The issue of signals towards the printer is conditioned by a particular logic to satisfy the following reasons:

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- 1 - The GE 130 Status 02/03 is equivalent, for the GE 115 1 and 2 to Status 119. This status is repeated as many times as are the columns of the printer at about 6 us intervals, to explore all the memory position relative to a printed row and compare them with the pertinent photodisc code.
- 2 - For every position explored, a TU04 is issued which caused the printer column counter to evolve sequentially.
- 3 - If the contents of the memory at a particular address, is identical to the photodisc code, a TU02 is issued in addition to the TU04. This enabled the drive of the interested printing hammer.

The GE 130 has different requirements as to what explained above, so the behaviour is so modified:

- 1 - Channel 2 has least priority. Therefore if requests for channel 1, 2 and 3 are all present together, channel 1 requirements will be satisfied first, then those of channel 3 and only after these two cycled have been fully satisfied will the cycle on channel 2 be considered.
- 2 - For alignment requirements the TU041, with possible TU02e, must maintain a fixed frequency. This frequency could be of 2 us but, in conformity to what mentioned at point 1 (channel 2 min priority) it has been fixed to 6 us.

From what mentioned appears it appears as necessary to introduce a buffer between the memory reading logic and the comparison logic. This is because the memory may be scanned in an asynchronous fashion if the operation is in overlap mode and because a synchronism of 6 us is to be maintained. The buffer must be such as to memorize the quantity and the outcome of the memory scan comparisons.

It is useful to repeat that the memory is scanned with a completely random rhythm.

If the machine is not working in overlap, a logic is necessary to inhibit channel 2 cycle requests,

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and consequently further scans, when this 2 position buffer becomes full. In fact, in this case scans would occur every 2 us. while the results would be fed to the printer every 6 us. This would entail data loss.

Therefore, the TU04 and TU02 issue logic behaves in the following manner:

- a - Every time Status 0/2 0/3 is done the "load printer buffer" command (CE16) is issued. This command causes a +1 count in the buffer (or counter) which consists of flip-flops RICO and RICI (142-7-18).
- b - The buffer will count -1 every time a TU04 is issued to the printer. It therefore memorizes the number of characters compared for which no TU04 has been issued to the printer.

The counter initially evolves in the following manner:

	RICO	RICI
Initial condition	0	0
After 1st CE16	1	0
After 2nd CE16	0	1

Under these conditions the RICI at 1 generates RUC01 at zero (143-12) for which RIMZA goes to one and no further request for channel 2 is made. Flip-flop RICI when at one also sets FF RICS (145-13) the purpose of which is to enable the count of counter RUC0 - RUC1 (144-3-6). Count occurs at every TI10 clock.

This two flip-flop counter will count by threes up to the end of the scan of the printed row, thus giving out the 6 us frequency necessary for the issue of the TU04s.

So, when RICI1=1 at every 6 us a TU04 is issued (145-6).

If flip-flop RINO1 is in set the TU02 is also issued.

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The purpose of flip-flops RINO and RINI (144-21-24) is to store the information relative to the equality of the character withdrawn from memory and to synchronize the issue of the possible TU02 with its partner TU04 belonging to that particular printed row.

Actually, in the event that equality is reached (UAZ06=1), either RINC (RN20A=1 / 145-23) or RINI is set (RN21A=1 / 145-20) depending upon the configuration held by the RICO - RICI buffer. If the machine is operating in overlap, the memory scan (CE16) can bring RICO-RICI from the 00 configuration to that of 10 or from 10 to 01.

- In the first case, the result of the comparison will necessarily be coupled up to the 1st TU04 issued, for which reason it will be stored in RINO.

- In the second case, the result will be tied to the 2nd TU04 and thus stored in RINI.

At the issue of the first TU04 (with RICI1.TI10. RINI1.RINO1) (149-19), RINI is shifted into RINO thus conditioning the TU02 belonging to the second TU04. When the TU04 is issued, through RTO4 (145-2) signal REMIA (142-19) is obtained which causes RICO-RICI to count -1.

RICI1 and RINZA go to zero and a fresh cycle request for channel 2 is done so to again load RICO+RICI and, if necessary RINC-RINI.

The scanning of a printed row continues as previously described until the printer issues signal PINA, with end of row meaning.

Flip-flop HUK2 is set through signal FF21A (143-1) and a Status OA is done. This flip-flop can also be set if the memory addresser has reached the 164th scanned position without receiving signal PINA through RFO4A=0 (VOZ41.CE161 / 143-3).

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During Status OA, the following occurs:

- The least meaningful part of VA is zeroed to reset itself at the start of the row.
- Flip-flop REAB1 is reset, by the End-of-Print signal. (CE17) through REB1A (143-11) which clamps signal RIMZA to "1". No further cycle requests on channel 2 are initiated. The Processor then waits for the next printer photodisc code.

As the new photodisc code comes in, new channel 2 requests are made as seen previously.

Status OE is done.

The new photodisc code is recorded in RI and in the 1st position of the printed row.

Status O6 is then done.

During this status a comparison is done between the new photodisc code and the contents of the 2nd position of the printed row which now contains the 1st photodisc code forwarded by the printer. If the two codes do not give equality, the printed row is scanned again with the same procedures seen before.

If the codes are the same, it means that all possible configurations of the photodisc have been taken in consideration.

Flip-flop SIOO is then set to enable the issue of signal FIRU during the execution of Status OB. Status O3 is done.

This Status does not carry out any meaningful operation and is only a step through to Status OB by means of SA00 at 1.

The issue of FIRU (CE15) generates signal PAK5A = 0 (160-2) which sets flip-flop FEC2 (137-9) which, in turn, resets the channel 2 selection flip-flop FUC2.

Through the End-of-Print command CE17, further requests for cycles on channel 2 are inhibited (REB1A/143-11). REAB1 goes in reset (143-14) and RIMZA goes to "1".

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If the Processor is working in overlap on channel 1, the end of transfer on channel 1 is waited for and a Status B8 is done. During this Status, with condition DU98 (PC01.FUC2.RAS1) active, Statuses EA and EB are entered. If not in overlap, a Status B8 is immediately carried out and, during this Status, with condition DU97 (LU00.FUC2), the sequence goes to the alpha phase of the following instruction.

NOTE: Signal REDOA at zero prevents the issue of the TU04s if the RICO-RICI buffer is empty (0-0) and if there is no cycle under way on channel 2 (RES2).

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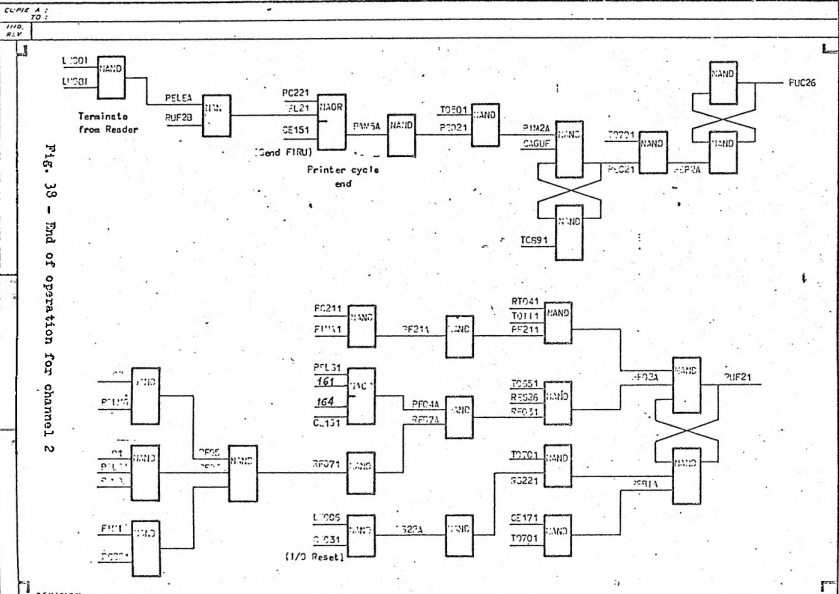
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9.9. Disparity error on channel 2

Disparity errors on photodisc codes from integrated printer are stored in flip-flop ERAR (143-17).

Set conditions are:

- RES26=1 Cycle attributed to channel 2
- PEST1=1 Check error found and enabled to the set of external error.
- TO891=1 Timing.

Flip-flop ERAR is reset by the signal REFUA=0 (143-8), signal which is either generated during Status CA in the general beta phase belonging to an instruction on channel 2, or by signal CAGUF at zero.

9.10. Channel selection logic

Bits 00 and 03 of L2, identify the channel to be selected. L2 contains the Z character. The following decodings are obtained:

- PC01 (128-8) - for channel 1
- PC03 (128-10) - for channel 3

Selection of channel 2 is done with bit L2 00 at 1. These decodings are stored in the channel selection FF's with the following timing logic:

PUC1=1 (136-3) Selection channel 1.

It is unconditionally set by command GEO2 which enables the channel selection even if the interested channels are 2 or 3. Flip-flop PUC1 is used during the general β phase for command forwarding or condition exam.

When a character transfer, in output, has been initiated with channel 1, signal PAP4A (136-21) resets PUC1 at the Start of the transfer phase exactly when the first transfer is done from RO into RA (CE00) unless signal PAR21 had already absolved this function.

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Signal PAR21 (137-6) is generated by command CI391, which is issued during the Status EO of the α phase of the following instruction.

For a TPER on channel 1 or a TPER on channel 2 in executive mode, PUC1 remains set either until the end of the instruction on channel 1 or up to the α phase of the following instruction.

Signal PIMIA, which is in OR with PUC16, is used to generate a small delay between the arrival of the reset command for PUC16 and the actual reset of it, to comply with some interface requirements. The same procedure is adopted for the selection of channel 3.

RASI=1 (136-12) Channel 1 in transfer.

This flip-flop is set at the end of the general β phase, by the command "Set I/O" (CE07) if channel 1 is to be selected (PC016). It is reset by the end of transfer condition on channel 1 (PAP3A).

PUC2=1 (136-18) Channel 2 in transfer.

This flip-flop is set, at the end of the general β phase, by the command "Set I/O" (CE07) with the presence of condition L2 006. It is reset by the end of transfer condition on channel 2 (PEC21).

PUC3=1 (136-29) Channel 3 in transfer.

It becomes set, at the end of the general β phase, by command "Set I/O" (CE07) if channel 3 is to be selected (PC036). It is reset by the end of transfer condition on channel 3 (PEC31).

The conditioning of PIM3A occurs in the same way as per channel 1.

9.11.

Connector selection logic

During the general β phase, at Status D8, signal AEBE is forwarded to the Peripheral Unit to be selected by means of command CE02. This command accompanies the unit selection character.

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Bits LIO7 and LIO6, belonging to the connector selection code, are stored at the same time as above in the following flip-flops:

- 1) PB07 (134-3) and PB06 (134-9). Unconditionally. These two flip-flops are used to supply the connector selection during the general β phase. They also supply selection during transmission on channel 1.
- 2) PB26 (134-18). If channel 2 is considered. It is to be remembered that channel 2 can operate only with connectors 1 and 2.
For this reason, only bit 06 is stored, being the only bit that differentiates the two connectors.

- 3) PB37 (134-6) and (PB36 (134-11). If channel 3 is considered.
Flip-flops PC11 through 4, PC21 through 2 and PC31 through 4 furnish the decodings relative to coupling of connector to channel (Chap. 135). Through these decodings a selection level is obtained for the interested connector.

During the general β phase, signal PUC2 for channel 2, and PUC3 for channel 3, are missing. During this phase, the selection of the connector is obtained through the selection of channel 1, which occurs unconditionally and always supplies signals PC11 through 4.

9.12.

Connector busy logic (Chap. 134)

During the general β phase, Status CB, the selected connector is examined for the busy condition.

If the connector is still busy on a previous instruction, signals SEPE1, PU002, PU003 and PU004, with connector selected meaning, are active. Under these conditions, signal PUB06 goes to 1 (through 134-10, or 134-19, or 134-22) having, in fact, the meaning of connector selected.

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9.13.

Register RE

The register RE consists of 8 bits +1 check bit. It receives the contents of RO register through command CEO1 in the presence of strobe FIFO.

The register RE holds all the data that must be forwarded to the interested peripheral during:

- the initial phase of the instruction TPER (whatever the channel may be).
- The data transfer phase on channel 1.
- The execution of instructions CPER, EPER, SPER and LPER.

9.14.

Register RA

It consists of 8 bits +1 check bit. It is loaded with the contents of RO with command CEO0 in the presence of timing strobe FIFO. RA register, first, deals with the byte of the data transfer command for channel 3 towards the Peripherals interface, and then with the data exchanged in output through channel 3.

9.15.

RE and RA registers disparity bit

Registers RE and RA receive, during the data exchange in output, the information read from memory that must be sent to the Peripherals.

Signal ROP81 (135-5) is generated as a function of RO08F. When the Peripherals name to be selected is forwarded, the character under exam is contained in L1₂₁ (the 8 least significant bits). It is therefore necessary to generate the 9th bit for disparity.

To this purpose, flip-flop RECE (135-4) is set with command CEO2, issued during the general β phase, Status D8, if the check network finds a disparity error in RO (GEST1=1).

This means that the check bit must be at 1, therefore signal RECEA at zero forces ROP81 at one.

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CONF. IJ

CONF. IK

CONF. IL

CONF. IM

CONF. IN

CONF. IO

CONF. IP

CONF. IQ

CONF. IR

CONF. IS

CONF. IT

CONF. IU

CONF. IV

CONF. IW

CONF. IX

CONF. IY

CONF. IZ

CONF. JA

CONF. JB

CONF. JC

CONF. JD

CONF. JE

CONF. JF

CONF. JG

CONF. JH

CONF. JI

CONF. JJ

CONF. JK

CONF. JL

CONF. JM

CONF. JN

CONF. JO

CONF. JP

CONF. JQ

CONF. JR

CONF. JS

CONF. JT

CONF. JU

CONF. JV

CONF. JW

CONF. JX

CONF. JY

CONF. JZ

CONF. KA

CONF. KB

CONF. KC

CONF. KD

CONF. KE

CONF. KF

CONF. KG

CONF. KH

CONF. KI

CONF. KJ

CONF. KK

CONF. KL

CONF. KM

CONF. KN

CONF. KO

CONF. KP

CONF. KQ

CONF. KR

CONF. KS

CONF. KT

CONF. KU

CONF. KV

CONF. KW

CONF. KX

CONF. KY

CONF. KZ

CONF. LA

CONF. LB

CONF. LC

CONF. LD

CONF. LE

CONF. LF

CONF. LG

CONF. LH

CONF. LI

CONF. LJ

CONF. LK

CONF. LL

CONF. LM

CONF. LN

CONF. LO

CONF. LP

CONF. LQ

CONF. LR

CONF. LS

CONF. LT

CONF. LU

CONF. LV

CONF. LW

CONF. LX

CONF. LY

CONF. LZ

CONF. MA

CONF. MB

CONF. MC

CONF. MD

CONF. ME

CONF. MF

9.16.

NE A/O network

The AND/OR network NE consists of 9 bits. All the information that the Peripherals send to the Central Processor memory (through register RO) during the data exchange phase, go through this A/O network. Data come from the 4 connectors and are enabled into NE by means of appropriate conditionings.

- a) - Connector 1 - Photodisc codes (FU00 through 08) transit through this connector and go into NE if the cycle has been assigned to channel 2 (RES2) when the MZ4 is connected to it (PC21).
- b) - Connector 2 - Characters read from cards go through this connector. Enable is given by logic expression RES1.PC12+RES2.PC22+RES3.PC32. The card reader can in fact transmit data with all 3 channels.
- c) - Connectors 3 and 4 - Information coming from connectors 3 and 4 are enabled in NE with the following logic expressions:

RES1.PC13+RES3.PC33 - Channel 3

RES1.PC14+RES3.PC34 - Channel 4

Connectors 3 and 4 can perform data transfers connected to either channel 1 or channel 3.

9.17.

Condition exam network

The condition exam network examines the interface conditions of the selected connector.

The exam condition is established by the configuration held in RO.

The condition exam network may be used as follows:

- 1 - During Status DC of the general β phase RO register becomes loaded, through a forcing step, with the configuration 0/1 which corresponds to the configuration of unit free exam condition (PE00). Thus the condition exam network gives the availability of the selected peripheral.

COMPL. 1
TUB. 1
REF. 1

COMPL.

APPL.

UNIT

SEC. S.P.S. - GEISI

N° 30004122 o/A

EMISS.

27/1/69

Pm

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CONT. SU FO. 240 NO. 239

2 - During Status CC, the register RO receives the subfield character X.

Therefore for an EPER, flip-flop FA05 stores either the presence or the absence of the condition under exam through signal PCOV.

The condition exam network is made up of:

- a logic network to decode the configurations held by RO. Outputs are RG00 through RG14
- a logic network to select the interface information depending upon the selected connector
- a logic network to make a comparison between the decoding of RO and the information present on the interface. Outputs PCOA through OL are in OR to generate signal PCOV6 which has the meaning of condition occurred.

CONT. A
IND
REV
FO. 57

REVISION

COMPL

APPR

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S.P.S. - GEISI

N° 30004122 o/A

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CONT. SU FO. 241 FO. 240

GE 130 - P.D.S.

1st APPLIC.

CONT. SU FO. 242 FO. 241

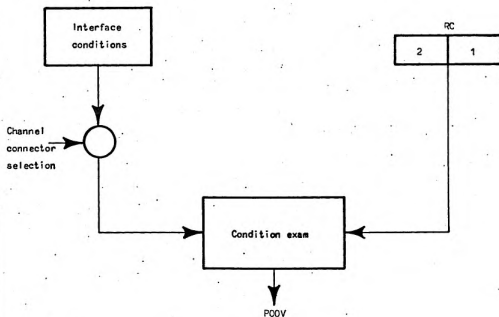


Fig. 39 - Condition exam network

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CONT. SU FO. 242

FO 241

GE 130 - P.D.S.

1^{re} APPLIC.

CONT. SU FO. 243 FO. 242

The following table shows the equivalence between:

- the configuration held by PO
- the condition that must be examined
- the corresponding decoding of RO which is activated.

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n° 30004122 o/A

CONT. SU FO. 243 FO. 242

GE 130 - P.D.S.

IF APPLIC.

CONT. SU. NO. 244 FO243

Unit in HO		Name of Condition	Enabled decoding	M E A N I N G				Serial Print. (Connector 1)
				Standard (connector 3/4)	Integ. Reader. (Connector 2)	Paral. Integ. Print. (Connector 1)		
01	PE00		RG00	Unit available				
03	SDGE		RG01	External error	Read error	-	-	
05	FISE		RG02	Not defined (3)	End of flow	End of form	-	
08	EGOL		RG03	Not defined (3)	-	End of form (1)	-	
10	MAPE		RG04	Not defined (3)	-	-	-	
12	TESE		RG05	Not defined (3)	-	Paper low (2)	Not defined (3)	
14	MARE		RG06	Out of service				
1A	MATE		RG07	Not defined (3)	-	-	-	
1E	CAPE		RG08	Command or data rejected	-	-	-	
22	IGOL		RG09	Not defined (3)	-	-	-	
24	MU10		RG10	Not defined (3)	-	-	-	
2A	MU20		RG11	Not defined (3)	-	-	-	
2C	MU30		RG12	Not defined (3)	-	-	-	

REVISION

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CONT. SU. NO. 244 NO. 243

Cod. 35/128 9

COMPL.		APPR.		UNIT		REV.		S.P.S. - P.D.S.		CONF. SU. PO. P. 244	
DATE		SIGNATURE		LOCATION		REVISION		MEANING		CONF. SU. PO. P. 244	
Unit in EO	Name of Condition	Enabled decoding	Standard (Connector 3/4)	Integ. Reader. (Connector 2)	Faral. Integ. Print. (Connector 1)	Serial Print. (Connector 1)					
2E	SECO	RG13	Manual								
42	ERCA+ Parity error in input	RG14	Transfer error	(4)	Photodisc parity error	Transfer error					
44	Abnormal Conditions	RP20	OR of Tests 03,05,08,12,14,1E,42	OR of Tests 03,05,14 (4)	OR of Tests 05,08,12,14,42	OR of Tests 12,14,42					
4A	Errors	RP30	OR of Tests 03,42	Equivalent to Test 03 (4)	Equivalent to Test 42	Equivalent to Test 42					

NOTES:

(1) - Only for double tractor printers.

(2) - For double tractor printers. Referred to 1st tractor unless special selection has been made for 2nd.

(3) - Variable meaning signal depending on Peripheral type.

(4) - Parity error in input is associated with the channel and never generated by integrated reader. Never active, if program is correct, for reader condition requests.

22 / 1 / 63

S.P.S. - GEISI

Pregnana

30004122 o/A

CONF. SU. PO. P. 244

GE 115/3 -120-130

CPU-POWER SUPPLY-CONSOLE

SUBSYSTEM

Installation

Second edition



[illegible]

Mod. 075

GE 115/3 - 120 - 130

4.571.0.002.2/A

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1. INTRODUCTION

The purpose of this manual is to outline the operations required to install the following subsystems :

130 A16-A24-A32	{	Central Processor	(Wing C) - 8K-12K-16K-24K 32K - 50/60 Hz
120 A12-A16-A24		Power Supply	(Wing D) - 50/60 Hz
115/3 A8-A12-A16		Console	(Wing F)
		Power Supply Extension	(Wing E) - See par. 10
		Memory Extension	(Wing M) - See par. 11

The hereby set out description presumes that the site has been adequately prepared according to the requirements quoted in the "Site Preparation" manual, but do not directly consider the single system configuration; in-fact, the installation engineer and/or team will draw all the necessary details from the following 2 auxiliary documents, individual to each installation :

a) - Site Layout

Giving the collocation of the subsystems in the site and showing those accessories which, though not normally supplied with the subsystems, are necessary to overcome particular space or operative problems. (i.e. - extra low level cable ducts, etc.).

b) - Unified Subsystem Connections (USC)

The forms bearing the above name give information upon the connection of the subsystem to :

- . CPU or MPA connectors
- . AC supply breakers
- . centralized DC Power Supply
- . fan supply and control terminal strip
- . AC supply control circuit

A detailed description on how to use the USC forms, which also give details on the insertion of calibration plugs and terminator boards, will be found in par. 1.1.

The final subsystem check-out must only be carried out if all the system structural and electrical connections have been completed and if the CPU and program loading subsystem check-outs have been accomplished.

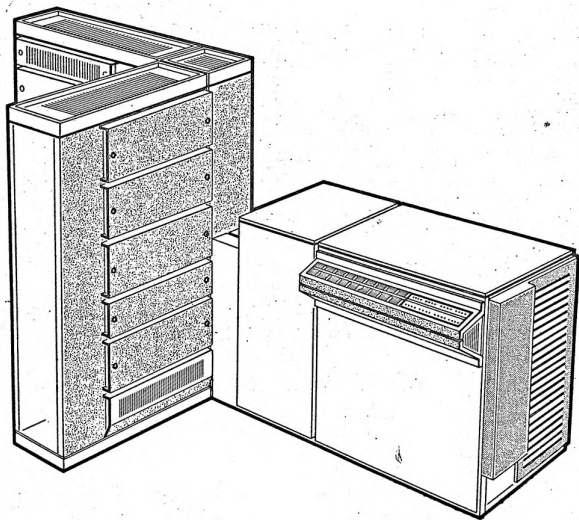


Fig. 1.1. - Composition of the 3 Wings - C, D and F

1.1. - "USC" FORMS

The Unified Subsystem Connections forms are two in number and present themselves under table form.

It is compiled by the Refurbishing and Site Preparation Bureau.

The various boxes and tables making up the forms bear cross-references to the "Cable lists for physical units" whenever reference is made to variable connections.

The purpose of the USC forms is to make more easily comprehensible the connections, positionings and symbolic markings on the cable ends.

Hereby following are given some examples to ease their interpretation:

Note

If the symbolic marking on a given cable is:

U - CPU - +20 V

it means that the cable comes from the "CPU" and goes to table "U" of the USC form and is a "+20 V" cable.

CABLES AND LOGIC PLUGS INSERTION

(TABLE "L.")

CONNECTOR 1				CONNECTOR 2				CONNECTOR 3				CONNECTOR 4				
SUBSYSTEM NAME 192				SUBSYSTEM NAME 128				SUBSYSTEM NAME 0 to 63				SUBSYSTEM NAME 64 to 127				
SUBSYSTEM NAME	UCE 460 POSIT.	CORN. SUBSYS.		SUBSYSTEM NAME	UCE 460 POSIT.	CONNECTED SUBSYSTEM		SUBSYSTEM NAME	UCE 460 POSIT.	CONNECTED SUBSYSTEM		SUBSYSTEM NAME	UCE 460 POSIT.	CONNECTED SUBSYSTEM		
A	H 03		<input checked="" type="checkbox"/>	O 01		CRZ		H 01		MPA		N 03		X		
B	K 03			M 01				H 02					N 01		X	
C	L 03			L 01				L 02					N 02		X	
D	L 03							I 02					M 02		X	
E	T 03							G 01				G 02		X		
PRT				CRZ				MPA				PTR				
1				2				2				2				
TAP C				TAP C				TAP C				TAP A				
MPA 130 (WING F MPA 130)																
CONNECTOR 1				CONNECTOR 2				CONNECTOR 3				CONNECTOR 4				
SUBSYSTEM NAME				SUBSYSTEM NAME				SUBSYSTEM NAME				SUBSYSTEM NAME				
SUBSYSTEM NAME	NPA 130 POSIT.	CONNECTED SUBSYSTEM		SUBSYSTEM NAME	NPA 130 POSIT.	CONNECTED SUBSYSTEM		SUBSYSTEM NAME	NPA 130 POSIT.	CONNECTED SUBSYSTEM		SUBSYSTEM NAME	NPA 130 POSIT.	CONNECTED SUBSYSTEM		
A	P 10		<input checked="" type="checkbox"/>	Q 14				Q 20				R 24		X		
B	P 10			Q 15				Q 21				R 25		X		
C	P 12			Q 16				Q 22				R 26		X		
D	P 13			Q 17				Q 23				R 27		X		
E	P 14			Q 18				Q 24				R 28		X		
MTC								JSU				CTN				
TAP A				TAP A				TAP A				TAP A				
CPU 130 ENABLE INTERRUPTION																
5 NO				3				5 YES				4				
POSITION				TYPE				POSITION				TYPE				
UCE 450 F 04				PORT 2P				UCE 460 F 04				TYPE				
ENABLE CPU130 CONNECTORS TO INTERRUPTION IF CPU130 HAS INTERRUPTION ENABLED																
<input type="checkbox"/> CONNECTOR 3 and 4				<input type="checkbox"/> CONNECTOR 3				<input checked="" type="checkbox"/> CONNECTOR 4								
POSITION				POSITION				POSITION				POSITION				
UCE 450 F 03				UCE 450 F 03				PORT 2N				UCE 450 F 03				
MPA 130 CONNECTORS WITH INTERRUPTION ENABLED																
(For operations to be performed refer to dwg n° 140242790)																
CONNECTOR 1				CONNECTOR 2				CONNECTOR 3				CONNECTOR 4				
<input checked="" type="checkbox"/> YES <input checked="" type="checkbox"/> NO				<input checked="" type="checkbox"/> YES <input checked="" type="checkbox"/> NO				<input checked="" type="checkbox"/> YES <input checked="" type="checkbox"/> NO				<input checked="" type="checkbox"/> YES <input checked="" type="checkbox"/> NO				
CPU130 CONNECTORS ENABLED TO PROGRAM LOADING																
<input checked="" type="checkbox"/> CONNECTOR 2 and 3				<input checked="" type="checkbox"/> CONNECTOR 4 and 2				<input type="checkbox"/> CONNECTOR 3 and 4								
POSITION				POSITION				POSITION				POSITION				
UCE 450 E 04				UCE 460 E 04				PORT 2N				UCE 460 E 04				
NOTE: - <input checked="" type="radio"/> Plug to introduce if parallel printer connected																
<input checked="" type="radio"/> Plug to introduce if subsystem connected with 3 cables																
<input checked="" type="radio"/> Board already inserted																
<input checked="" type="radio"/> It is necessary to take out board from position given on table																

TABLE "L"

- Gives the informations necessary for logic connections and insertion of calibrator plugs.
- 1 - Relationship between the symbolic name on signal cables and the true location of UCE 460 connectors.
- 2 - Name of the subsystem connected to the interested UCE 460 connector.
- 3 - The cross shows the type and position of calibration plugs to be fitted. See Note for further details.
- 4 - The cross gives fitment of MPA in the system. Interpret table as per UCE 460.
- 5 - Cross in correspondance to YES or NO shows whether interruption is or is not enabled. See Notes 3 and 4 for details.
- 6 - If interrupt is enabled, cross shows which connector and what plug is to be fitted. Example shows connector 4 and board PONT 2P is to be fitted in slot F 03.
- 7 - If MPA is fitted, cross on YES or NO gives changes to be done, with aid of Dwg. 14024279.0 Sheet 2, on board FACI in slot O-3g of MPA 130.
- 8 - Cross determines the type of program loading chosen and gives type and position of relative plug.
- 9 - Relationship between name and Part Number of plugs.

CABLES AND A.C. BREAKER INSERTION (TABLE "T.")													
50 Hz WING B ALI 260 - 2nd													
SYMB. NAME	X	Y	Z	N	GR	SYMB. NAME	X	Y	Z	N	GR		
POSIT.		BREAKER 1				POSIT.		BREAKER 3					
CONN. SUBSYS.						CONN. SUBSYS.		PTR					
OUTPUT BR1 =						OUTPUT BR3 =		2					
CONN. SUBSYS.		CRP				CONN. SUBSYS.							
POSIT.		BREAKER 2				POSIT.		BREAKER 4					
SYMB. NAME	X	Y	Z	N	GR	SYMB. NAME	X	Y	Z	N	GR		
OUTPUT BR2 =		5,5				OUTPUT BR4 =							
TOT. OUTPUT BR1 + BR2 + BR3 + BR4 =						7,5		≤ 30 A					
50 Hz WING B ALI 260 - 1st													
SYMB. NAME	X	Y	Z	N	GR	SYMB. NAME	X	Y	Z	N	GR		
POSIT.		BREAKER 1				POSIT.		BREAKER 3					
CONN. SUBSYS.		PRT				CONN. SUBSYS.		CPU1					
OUTPUT BR1 =		5				OUTPUT BR3 =		9,5					
CONN. SUBSYS.		CRZ				CONN. SUBSYS.		CPU2					
POSIT.		BREAKER 2				POSIT.		BREAKER 4					
SYMB. NAME	X	Y	Z	N	GR	SYMB. NAME	X	Y	Z	N	GR		
OUTPUT BR2 =		3				OUTPUT BR4 =		5					
TOT. OUTPUT BR1 + BR2 + BR3 + BR4 =						22,5		≤ 30 A					

TABLE "T."

- Shows connections to be done for AC supply connections and for the insertion of breakers.
The location of the breakers and of the ALI 260 on Table "T" reflects the actual position of the same in Wing B.

- 1 - Name of the subsystem whose AC supply cable is to be connected to the relative breaker.
- 2 - Position of terminals XYZ of interested breaker. Terminals, as per form, may be positioned either toward the bottom or the top depending upon the position of breaker fitment.
N and GR (Neutral and Ground) are buss bars.
N is above breakers 1 and 3, GR below breakers 2 and 4.
- 3 - Total AC current output of interested subsystem.

Note
Terms CPU 1 and CPU 2 are referred to an SCR 130 A Power Supply, of which the first module (CPU 1) is supplied by breaker 3 and the second (CPU 2) by breaker 4.

- 4 - Max. output current is 30 A for 50 Hz and 27 A for 60 Hz versions.

D.C. CABLES INSERTION				(TABLE "U")				
WING D ALI 031				WING E ALI 031				
+20	SYMBOL NAME	TER., BOX POSIT.	CONN. SUBSYS.	ABS. D.C. SUBS. (A)	SYMBOL NAME	TER., BOX POSIT.	CONN. SUBSYS.	ABS. D.C. SUBS. (A)
			PTR	6			MTC	14.5
			CRP	12.5				
			2	4				
	OUTPUT P7 - 1 =		18.5	≤ 40 A	OUTPUT P7 - 1 =		14.5	≤ 40 A
	TER. BOX POSIT.	CONN. SUBSYS.	ABS. D.C. SUBS. (A)	TER. BOX POSIT.	CONN. SUBSYS.	ABS. D.C. SUBS. (A)		
		CPU	4.6		PRT	9		
		MPA	5.8					
		CRZ	8					
	OUTPUT [P7 - 3] =		34.5	≤ 40 A	OUTPUT [P7 - 3] =		9	≤ 40 A
	TOTAL OUTPUT [P7 - 1] + [P7 - 3] =		53	≤ 65 A ≥ 13 A	TOTAL OUTPUT [P7 - 1] + [P7 - 3] =		23.5	≤ 65 A ≥ 13 A
WING D ALI 032				WING E ALI 032				
MASSA	SYMBOL NAME	TER. BOX POSIT.	CONNECTED SUBSYSTEM	SYMBOL NAME	TER. BOX POSIT.	CONNECTED SUBSYSTEM		
			CPU			MTC		
			MPA				PRT	
			CRZ					
	[P7 - 2]	PTR	↑					
		CRP		6				
		5						
		WING D ALI 030 (-45)			NOTE: -			
	TERMINAL BOX POSITION	CONNECTED SUBSYSTEM						
	J4 - 10 - 1	7						

TABLE "U,"

- Gives informations about DC supply connections.

1 - Cross shows presence of second power unit (in Wing E) thus 130 A supply.

2 - Name of the subsystem whose DC supply cable (marked as +20) is to be connected to terminal board P7-1 of ALI 031 (First power unit).

2' - Name of the subsystem whose DC supply cable (marked as +20) is to be connected to terminal board P7-3 of ALI 031 (First power unit).

3 3' - As 2 and 2', but referred to the second power unit.

4 - Subsystem load.

5 - Name of the subsystems whose DC supply cable (marked as MASSA) is to be connected to terminal board P7-2 of ALI 032 (First power unit).

5 - As 5, but referred to ALI 032 (Second power unit).

7 - Name of the Data Transmission subsystem (if any) whose -45 supply cable is to be connected to J4 - 10 - 1 of ALI 030.

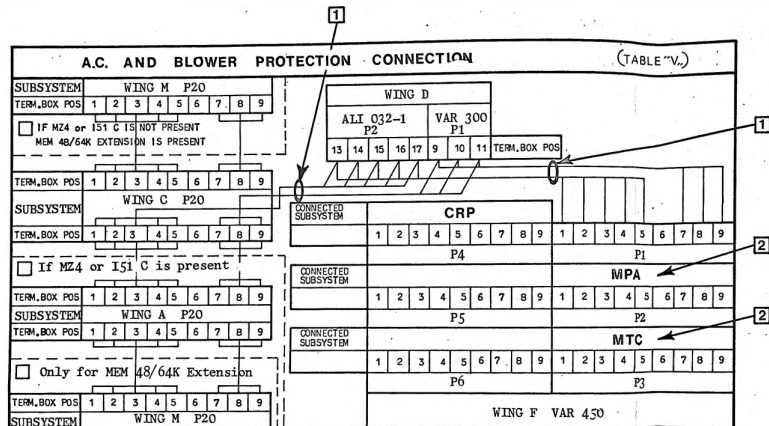


TABLE "V,"

- Gives information regarding the supply and control of blower groups.

- 1 - Standard connections to be done (clearly shown on cables).
- 2 - Name of the subsystem to be connected to relative terminal board on VAR 450 (Wing F).

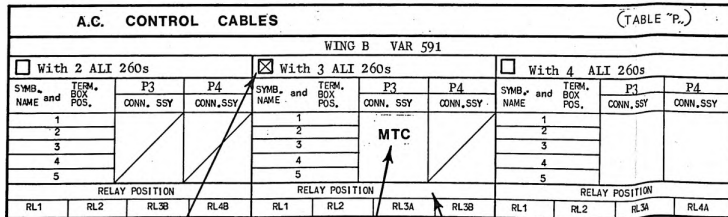


TABLE "P,"

- Gives information on connection of control cables between ALI 260 and VAR 591.

- 3 - Example shows that there are three ALI 260s in the System.
- 4 - Name of subsystem inclusive of one ALI 260 which is slaved to two ALI 260s fitted in Wing B through connection to VAR 591 terminal board P3.
- 5 - Location of relays on VAR 591 if three ALI 260s are fitted.

A.C. CONTROL PROTECTION CABLES CONNECTION - TABLE "M" -				
WING B VAR 591				
IF M.P.S. CONNECTED TO THE VAR 591 P4 T.BOX		IF M.P.S. CONNECTED TO THE VAR 591 P3 T.BOX		
SYMB. NAME	VAR 591 POSIT.	CONN. SUB.	VAR 591 POSIT.	CONN. SUB.
4	P2 - 4		P2 - 4	
R	P1 - 3		P2 - 5	

↑
3

↑
1

↑
3

↑
2

TABLE "M",

- Gives informations regarding the AC control when the MPS subsystem is connected.

- 1 - Name of the subsystem connected to the MPS if the MPS cable is connected to P4 T.S. of VAR 591
- 2 - As above, but when the MPS cable is connected to P3 T.S. of VAR 591
- 3 - Clamp position for "4" and "R" cables in case 1 or 2

2. TOOLS AND INSTRUMENTS

The operations to be performed for the installation may be carried out with the use of the following equipments:

- Engineer's tool kit,
- Tools for GE 115/3 - 120 - 130,
- Bushing type pliers (P.N. 4355406 G).

3. ACCEPTANCE AND COLLOCATION

3.1. - PACKING

The CPU, Power Supply, Operator Panel, Power Supply and Memory Extensions, with all their associated equipment and documentation, are normally shipped to their destination in two packages.

External to each packing crate, are affixed two forms giving:

- the contents of the crate,
- the guide to uncrate and remove from the pallet (*)

(*) - Wooden battened transport base.

3.2. - ACCEPTANCE

All packages are to be visually examined for damage. If any damage is noticed, it will be necessary to:

- have the carrier witness the entity of the damage,
- submit a detailed report to Headquarters.

3.3. - UNCRATING

- Ensure that the subsystems are uncrated adhering to the recommendations set down in the uncrating guide attached to the outside of the crate itself.
- Ensure that the contents tally with the description.
- Remove from the crates the documents and accessories therein contained and set them aside.
- Check that, for each subsystem, there is all documentation and diagnostic decks listed in the "System Composition Sheet". In case of any missing documents or diagnostics inform headquarters.

Caution

Great care is to be exercised when the wings are moved about so that they do not topple over.

3.4. - COLLOCATION

The machines are to be positioned as per Site Layout.

It is advisable to start the layout first placing the CPU, the SCR, the PRT, the console and so on.

4. MECHANICAL ASSEMBLY

Note

If the Power Supply Extension is fitted, also refer to par. 10. If the Memory Extension is fitted, also refer to par. 11.

- Take off all removable skins from Wing C, D and F.

Wing C and D

The panels covering the electronic modules can be removed through quick-release fasteners; the cable channel covers by withdrawing the upper pins.

Wing F

Lift the Formica top. The front and rear panels are to be pulled towards the outside.

- Wing C (CPU) to Wing D (Power Supply) junction (*)

Refer to Dwg. n° 15043900. Join the two wings by means of the two rings 1 and 2 and distance piece 7. The position of ring 1 may have to be adjusted when skinning up the machine.

- Console (Wing F) to Wing C and D junction (*)

Still referring to Dwg. n° 15043900, join Wing F to the lower ring 2 together with distance piece 7.

(*) - Should Wing F be envisaged in line with Wing C, refer to par. 4.2., if the Power Supply Extension has been foreseen the console cannot be in line with the CPU.

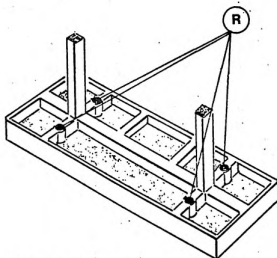


Fig. 4.1. - Base screw-feet

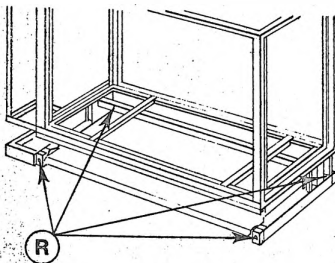


Fig. 4.2. - Plumb setting points

Note

During assembly, first withdraw the screw-feet (R) located at the base of the wings and of the console to set units plumb.

4.1. - DOUBLE FLOOR INSTALLATIONS

Whenever a system is to be installed in a double floor site, the below sequence is to be followed.

The exits for cables from the basic group (PRT - CPU - CRZ - CONSOLE) to the false floor are located and obtained as per layout below:

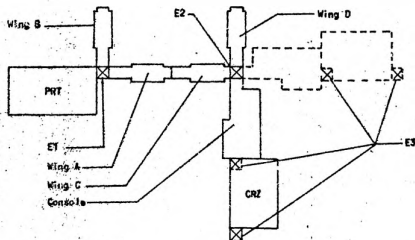


Fig. 4.3. - Double floor cable exits

- E1 and E2, are obtained by removing the bottom covers P.N. 0835835 F. See Dwg. n° 15043900.
 - E3, is obtained by placing in correspondence to the CRZ cable channel, when it is not fitted, the cabinet bearing P.N. 0674296 F.
- These exits are used for the following cables:
- E1 = AC supply and ALI 260 control.
 - E2 = DC, signals and supply for fans of subsystems connected to the CPU.
 - E3 = DC, signals and supply for fans of subsystems connected to the MPA.

The cable connecting the basic group subsystems, use the normal run inside the low level cable ducts.

It is advisable to have the AC and DC cables run parallel inside cable ducts when the system is installed in a double floor site.

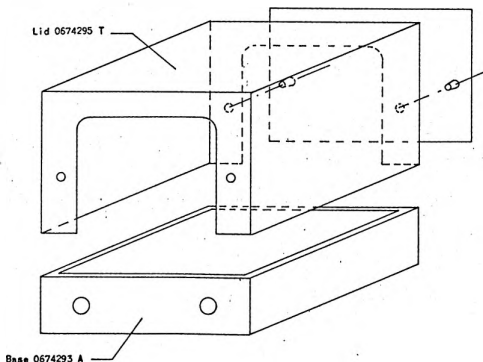
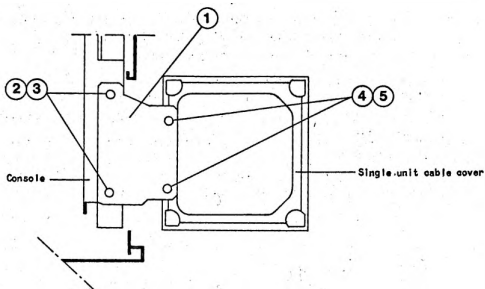


Fig. 4.4. - Cable cover single unit P.N. 0674296 F

N° 1 Closure plate 0674303 F

N° 1 Spring clip. Type SPF 2159 - 0834665 R



- | | |
|-------------------------------|-------------|
| 1 - N° 1 Plate Type A | - 0674306 C |
| 2 - N° 2 Screw, Allen M5 x 15 | - 6313132 B |
| 3 - N° 2 Washer 5,3 mm | - 6331105 T |
| 4 - N° 2 Screw, Allen M6 x 15 | - 6313148 W |
| 5 - N° 2 Washer 6,4 mm | - 6331106 F |

Fig. 4.5. - Mounting hardware for single unit to Console

4.2. - CONSOLE LINED UP WITH WING C

To position the console 90° off the normal layout with the CPU, the console is to be turned clockwise through 90° together with the junction rings to allow the fitment of covers. See Figs. 4.6. and 4.7.

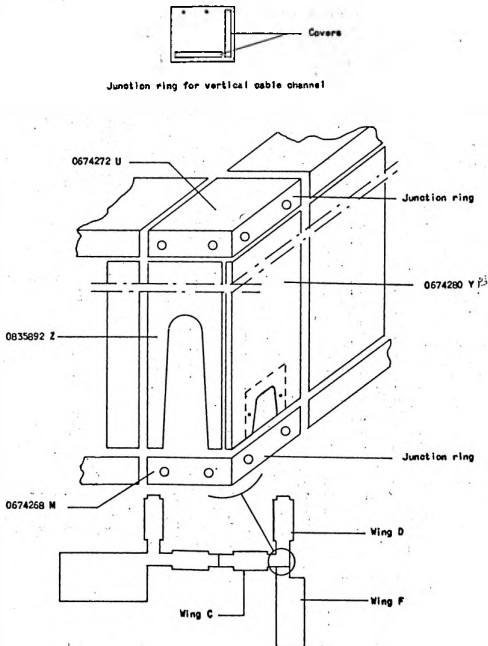
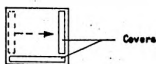


Fig. 4.6. - Normal position



Junction ring for vertical cable channel

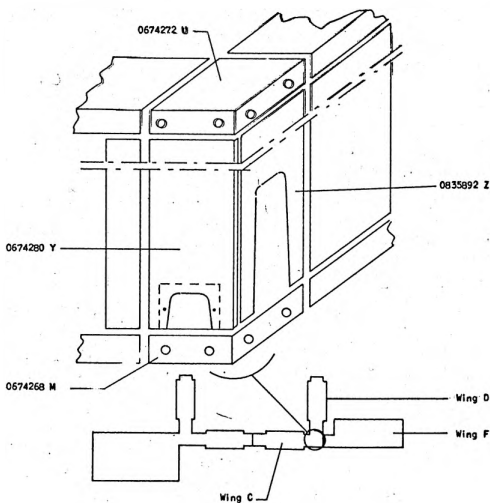


Fig. 4.7. - In line with CPU position

5. CABLE CONNECTIONS

Wing F

- Refer to Dwg. n° 15043017.
- Use cable kit 0646562 N. Lay the cables out and by following the markings on the cable ends, connect:
 - a - Signal cables (C2 to C5). Fit one end of the 4 AMP connectors (J2-J3-J4-J5) into the TAV 460 and the other end in the 10 cable connectors of the UCE 460; hence connect them up to their connectors starting from rows H-I-N.
 - b - Control cable (C6). From TAV 460 (J6) to Wing D, ALI 030 (J6).
 - c - DC cables (C7 - C8). From TAV 460 to Wing C (Table U of USC).
 - d - AC cables (C9 - C10 - C11). From VAR 380 to Wing D, ALI 030.
- If an MPA 130 is mounted, refer to relative Installation Manual and Dwg. n° 15043512 (Block schematic - Physical) for cables layout and to locate terminal boards, buss bars, etc.

Wing D

- Refer to Dwg. n° 15043008.
- Use parts kit 0646807 Q. Lay the cables out (One end is already connected to the Wing) and by following the markings on the cable ends connect:
 - a - Signal cables (C13) from ALI 290 to Wing B (see Table L of USC), feeding it through the side holes of the ALI 260, to connect up the AC supply. Connect C13 to the breaker and mount the latter in the ALI 260, securing C13 with Bushing clamp and pliers. See Fig. 7.2.
 - b - One cable (C14). From VAR 300 to Wing F, TAV 460.
 - c - Two cables (C15 - C16). From VAR 300 and ALI 032 to Wing C, VAR 321.
 - d - One cable (C17). From VAR 300 to Wing B, VAR 591.
 - e - Two cables (C18 - C19). From VAR 300 and ALI 032 to Wing F, VAR 450.
- When all the subsystems have been connected to the Wing, secure all cables by means of the nylon straps as shown in the physical block schematic of the single wings.

Wing C

- Refer to Dwg. n° 15043184.

- Lay the cables out and, by following either the real or the symbolic cable markings on the cable extremities, connect up the cable free ends.
 - a - Two cables (C3 - C4). From P1 to Wing D, ALI 150.
 - b - Two cables (C5 - C7). From P2 and P4 to Wing D (Table U of USC) for +20 VDC supply and ground.
 - c - Two cables (C6 - C8). From P3 and P5 to Wing D, ALI 150.
- Satisfy requirements set down in Table L of USC, by fitting plugs drawn from parts kit 0646542 L. Precisely:
 - a - Fit the required plugs to the CPU connectors.
 - b - If Interrupt is enabled, remove board PONT 2P from UCE 460 slot F-04.
 - c - If CPU Interrupt enabled, either fit or not, plug board in UCE 460 slot F-03 in correspondence to the enabled connector.
 - d - Either fit or not, board PONT in slot E-04, depending on the type of use envisaged.
- Secure cables with the provided plates and nylon thumb screws. Lay out cables along their run and secure them with the nylon straps as shown in the physical block schematics of the single wings.
- Carefully fit the required memory stacks.

Note

If ever difficulties are experienced in reading cable markings, the identification of these may be established by referring to the following drawings:

- Dwg. n° 15023048 - Console
- Dwg. n° 15023128 - Power Supply
- Dwg. n° 15023158 - Central Processor

6. VISUAL CHECKS

When all cable connections have been done, it is indispensable to carry out an accurate visual check to:

- The correctness of the mechanical assembly.
- The proper insertion of all boards, cable connectors and plugs.
- The wire-wraps, for loose wraps, bent pins or broken wires.
- The layout, the path and security of attachment of all cables.
- The presence of terminal strip covers and routing of cables to their appropriate terminal strips.
- The correct and square fitment of relays in Wing D (ALI 030-ALI 031-150) and possible Wing E (ALI 031).

7. WING B9/B INSTALLATION

Caution

If the installation of a basic system is to include Wing B9 (151 BGE printer), all what mentioned at para. 1, 2, 3, 4 and 4.1. is to be retained as valid with the addition of the following instructions.

7.1. - MECHANICAL ASSEMBLY

- Take off all removable panels.
- Refer to Dwg. n° 15043904. Join Wing B9/B to Wing C and D (already joined) using junction rings 1 and 2 and distance pieces 5.
- Refer to Dwg. n° 15043905 if low level cable ducts are to be fitted. Join them together and then to Wing B9/B as shown in the mentioned drawing.

7.2. - CABLE CONNECTIONS

- Refer to Dwg. n° 15043516.
- Follow marking (real) on the cables to connect Wing B ALI 260/1 with Wing F (TAV 420 P1) utilizing cable C1.
- Use the two AL 145 (C3 and C4) cables. The Hubbel end is to be inserted in the two ALI 260 J1; the other end in the mains supply.
- Insert the VAR 591 relays as shown in Table P of the USC form.
- Use Bushing cable clamps and pliers for all cables outgoing from the ALI 260s. See Fig. 7.2.

Note

If ever a cable is found without markings or they are indecipherable, reference to be made to Dwg. n° 15023532.

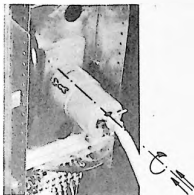


Fig. 7.1. - Fitment of a Hubbel plug

Caution

When a Hubbel plug is to be fitted, the following steps are to be adhered to:

- Make the reference marks coincide. See Fig. 7.1.
- Fully push home the plug into its socket.
- Rotate CW until the locking click is heard.

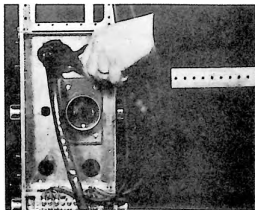


Fig. 7.2. - Use of the Bushing pliers

7.3. - VISUAL CHECKS

When all mechanical operations have been completed, carry out checks on the following:

- The correctness of the mechanical assembly.
- Correct cable layout without slack or kinks.
- Security of attachment of cables to terminal strips.
- The relays on the VAR 591 must be fully home.

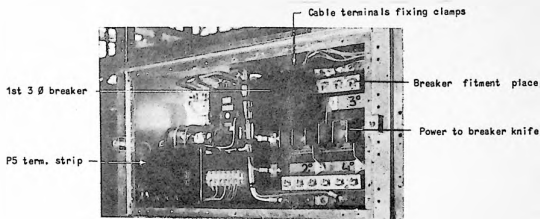


Fig. 7.3. - ALI 260 opened view

Note

Breaker n° 1 is partially fitted on the 3 power supply knives, where:

Phase X is black, Phase Y is red and Phase Z is blue.

8. CHECK-OUT




8.1. - OFF LINE CHECKS

- The AC mains supply must be switched off.
- Check by manually spinning the fans that they turn freely, without undue friction and that the stall vanes are perfectly free to move.
- Check that all the pushbuttons and switches on the Operator's Panel are serviceable.

Warning

The use of an A.V.O. meter must be limited to a type whose maximum potential between probes is not greater than 5 V, when set on the $\Omega \times 1$ range.
This is to prevent damage to the I.C. packages.

- Set meter to appropriate scale and measure for no shortcircuits between phases and ground (this check is to be effected both at the subsystems in put and on the various supply breakers in the OFF position).
- Set meter to the $\Omega \times 1$ scale and check, on terminal strip P2 of ALI 150 (Dwg. n° 15043008), for no shortcircuits between following DC voltages: +5, +12 and -20. Refer to table for values.

OHMMETER TERMINALS		VALUE FOUND	
(-)	(+)	Ω	*
	+12 V	9	
	+ 5 V	2,5	
-20 V		10	
+ 5 V	+12 V	14	
-20 V	+ 5 V	14	
-20 V	+12 V	36	

* - Approx. values

- Check for no shortcircuits between above mentioned voltages and the +20 VDC (P7-1 and P7-3 on ALI 031). Resistance value to ground is influenced by the number of subsystems connected. It must under no circumstance be below 0.3 Ω (if the SCR is at 65 A the resistance is 0.31 Ω).
- Before applying a.c. and d.c. power check that the ALI 150 +5 V, +12 V and -20V load switch jumper straps have been set to the Internal Load position.
Furthermore check that the ALI 150 current protection circuit shunt screws result completely loosened so as to avoid fall of the d.c. voltages on the Internal Load.
- Carry out the final check out on the peripherals as outlined in their pertinent manuals.

- Set all the ALI 260 and 280 breakers to ON.
- Set the switch at the foot of Wing D (VAR 300) to ON.
- Switch AC mains supply on.
- Press Operator panel pushbutton ~ ON.

8.2. - ON LINE CHECKS

- Check that the operator panel yellow POWER OFF light is lit.
- Check that the fans turn normally and without undue noise.
- If the fan protection circuit cuts in, set the switch on the VAR 300 to OFF and press ~ ON once more.
- Locate which fan group is defective and rectify the fault.
- Wait for about 20 secs (POWER OFF lit and DC ALERT out) before pressing POWER ON on Operator Panel. DC power is enabled.
- Check for nominal d.c. values on + 20V, -20V, + 12V and + 5V.
If two phases have been wrongly connected, the Power Supply protection circuit will intervene (*).
- After the checks on Internal Load have been duly carried out, switch the machine off, replace the load switch Jumper straps on their External Load position and fully tighten the appropriate ALI 150 current protection shunt screws.
- Press LAMPS CHECK. Ascertain that all operator and maintenance panel display lamps light except for those operated by pushbuttons.
For those associated with pushbuttons, press the appropriate STAND-BY, SWITCH 1, SWITCH 2, STEP-BY-STEP, LOAD twice (LOAD 1 - LOAD 2) pushbuttons, to obtain corresponding lamp light-up, and operate 1 of the maintenance panel slide switches for MAINT ON light-up.
- Run through the CPU and various subsystem diagnostics.
- When all the equipment has been checked, switch off the system through POWER OFF and EMERGENCY OFF. Spin up all subsystems.
- Switch the system back on and run through the SAT diagnostic program.

(*) - In case of irregular Power Supply operation, refer to the "Power Supply Intervention Procedures".

9. FINAL OPERATIONS

9.1. - CHECKS AFTER HANDOVER TO CUSTOMER

- Check that the type and serial number on the units yellow labels correspond to the description given on the "Product Composition Sheet".
- Transcribe on the "FCO Status Log", of the various Elementary Units, the drawing indices of all the documentation, comparing them with those given in the "Product Composition Sheet".
- Check that the tools and equipment supplied physically corresponds either to the packing list or the ISL recommended by the Headquarters.
- Prepare a Report giving details of snags or defects found during the installation.

10. POWER SUPPLY EXTENSION - WING E

When this extension is fitted, after paragraph 3.4., of this manual, also follow through the following points when on para. 4 and 5.

1) - Mechanical assembly

Take off the removable skins from wing E.

- Wing E to Wings C-D junction (use parts kit n°. 0696920 W)

Refer to Dwgs. 15043913 and 15043914. Join wing E to the upper and lower rings with distance piece 8. Care is to be taken in positioning the rings so as to enable the correct replacing of skin 3.

2) - Cable connections (use cable kit n°. 0646919 Y)

Refer to Dwg. 15043115. Lay out the cables to be connected, one end will already be connected to the wing, and following the markings connect:

- a - One cable (C1) from ALI 290 to wing B (Table "T" of USC form) feeding it through the pertinent ALI 260 side holes for the AC supply connection. Also connect up the breaker, inserting it in the ALI 260, and secure the cable with bushing clamp and pliers. See Fig. 7.2.
- b - One cable (C2) from ALI 032 to wing D - ALI 032.
- c - One cable (C3) from ALI 031 to wing D - ALI 030.

When all the subsystems have been connected to the wing, secure all cables by means of nylon straps.

Note

In difficulties in reading cable markings are encountered, it is possible to establish their identity by referring to Dwg. n° 15023136.

11. MEMORY EXTENSION - WING M

When this extension is fitted, after par. 3.4., of this manual, also follow through the following points when on par. 4 and 5.

1) - Mechanical Assembly

Take off the removable skins from wing M.

- Wing M to Wings A or B/9 and C Junction (use wing M parts Kit 0643440 G).
Refer to dwg. 78B103700 and join wing M to either wings A or B/9 and C, taking care to correctly insert the distance pieces.

2) - Cable Connections (use cable kit 0643439 A)

Referring dwg. 78B10305, lay out the cables to be connected (one end will already be connected to wing M) and, following the markings, carry out the connections shown on dwg. 78B103704.

When all cables have been connected, secure them along their path by means of their pertinent clamps.

Note

Should difficulties in reading cable markings be encountered, it is possible to establish their identity by referring to dwg. 70B103704.

11.3. - POWER SUPPLY

Follow the same general operations described in par. 11.1 to remove the Power Supply.

- Note that when removing the Power Supply, it is also necessary to disconnect the breakers from the ALI 260 (Wing B) and group the subsystem kit as specified in the Installation Manual.

11.4. - CONSOLE

Follow the same operations described in par. 11.1.

- During the removal of the console, the MPA 130, if present, must be securely fixed to the chassis as described in the pertinent Installation Manual.

12. SUBSYSTEM WITHDRAWAL

The following rules are to be applied when withdrawing a GE 115/3, 120 or 130 CPU subsystem so as to guarantee its completeness in view of possible further usage.

12.1. - REMOVAL

Care should be taken to control that every subsystem be complete of :

- All non implemented F.C.O.s, inherent material and documentation.
- Machine documentation with all revisions indicated on the FCO Status Logs.
- All initial spare parts and tool kits.

12.2. - CENTRAL PROCESSOR and POSSIBLE MEMORY EXTENSION

Referring to the appropriate chapters of this manual and the machine documentation, remove power from the subsystem and sequentially follow through the below listed operations :

- Deskin the CPU.
- Take off the vertical panels to ease removal operations.
- Disconnect signal, DC, AC and service cables to restore the subsystem in the conditions it was when initially received (only the ground and +20 V connections are to be left. All other cables are part of other subsystems).
- Extract the memory stacks (MEM 470), inserting them in the pertinent containers to avoid damage during transport.
- Proceed with all the necessary mechanical disassemblies, to permit movement of the subsystem to another area within the building, and prepare for shipment. During this operation, great care is to be taken not to damage the controller wing.
- Coil-up and secure all cables inside the subsystem so as to avoid damage during transport.
- Referring to the list of cables and parts necessary for the connections of physical units, group the material that is part of the subsystems kit and prepare it for shipment.

12.3. - POWER SUPPLY

Follow the same general operations described in par. 12.1 to remove the Power Supply.

- Note that when removing the Power Supply, it is also necessary to disconnect the breakers from the ALI 260 (Wing B) and group the subsystem kit as specified in the Installation Manual.

12.4. - CONSOLE

Follow the same operations described in par. 12.1.

- During the removal of the console, the MPA 130, if present, must be securely fixed to the chassis as described in the pertinent Installation Manual.

13. ATTACHED DRAWINGS

To complete the present Installation Manual, the following drawings are attached:

Name	Dwg. N°	Sheet N°
Cables and parts list to connect a physical unit - Console	15023048	
Cables and parts list to connect a physical unit - I51	15023086	
Cables and parts list to connect a physical unit - Power Supply	15023128	
Cables and parts list to connect a physical unit - CPU	15023158	
Cables and parts list to connect a physical unit - Wing B/9	15023532	
Block schematic - Layout - Power Supply	15043008	1 - 2
Block schematic - Layout - Console	15043017	1 - 2
Block schematic - Layout - CPU	15043184	1 - 2
Block schematic - Layout - Wing B/9	15043516	
Unit connection - Layout	15043900	1 - 2
Unit connection - Layout	15043904	1 - 2
Unit connection - Layout	15043905	1 - 2
Cables and parts list to connect physical units - Power Supply Extens.	15023136	
Block schematic - Layout	15043115	1 - 2
Unit connection - Layout	15043913	1 - 2
Unit connection - Layout	15043914	1 - 2
Mounting of wing M parts	78B103700	
Cable marking and connections - wing M	78B103704	
Cable installation - wing M	78B103705	

Note

The drawings herewith attached may not be continuously updated therefore, should incoherence be encountered, always refer to the machine documentation.

RIF REF	TIPO TYPE	MARCATURA CABLE LABELLING		FUNZ. FUNCT.	NOTE NOTES	RIF REF	KIT 1 COD. 0646562 N		KIT 2 COD.		DESCRIZIONE PARTI PARTS DESCRIPTION	KIT 1 COD. CODICE CODE		KIT 2 COD. CODICE CODE		NOTE NOTES
		LATO INT. ALL' U.F. SIDE INT. TO PH. UNIT	LATO EST. ALL' U.F. SIDE EXT. TO PH. UNIT				CODICE CODE	0	CODICE CODE	Q		CODICE CODE	Q	CODICE CODE	Q	
C2	NS 129	ALA F TAV 460 J2	ALA C UCE 460 M39		1	C2	0640151 N	2								
			ALA C UCE 460 M40		2	C3										
			ALA C UCE 460 L39		3											
C3	NS 129	ALA F TAV 460 J3	ALA C UCE 460 L40		1											
			ALA C UCE 460 L40		2											
			ALA C UCE 460 H40		3											
C4	NS107	ALA F TAV 460 J4	ALA C UCE 460 N39		1	C4	0640036 F	2								
			ALA C UCE 460 N40		2	C5										
C5	NS107	ALA F TAV 460 J5	ALA C UCE 460 I39		1											
			ALA C UCE 460 G40		2											
C6	NS128	ALA F TAV 460 J6	ALA D ALI 030 J6	Contr		C6	0640153 T	1								
C7	AL102	ALA F TAV 460 P2-3	U - CPU 3 +20	D.C.	4 - 6	C7	0640443 D	1								
C8	AL101	ALA F TAV 460 P2-1	U - CPU 3 MASSA	D.C.	5 - 6	C8	0640418 X	1								
C9	AL107	ALA F VAR 380 P1-3	ALA D ALI 150 P2-2	D.C.	4	C9	0640377 S	2								
C10	AL107	ALA F VAR 380 P1-1	ALA D ALI 150 P2-3	D.C.	4	C10										
C11	AL 103	ALA F VAR 380 P1-2	ALA D ALI 150 P2-4	D.C.	5	C11	0640F36 E	1								

- NOTE:
- 1) La marcatura va messa in corrispondenza del connettore GEISI contrassegnato con "1"
The marking must be set in correspondence of the GEISI connector labeled with "1"
 - 2) La marcatura va messa in corrispondenza del connettore GEISI contrassegnato con "2"
The marking must be set in correspondence of the GEISI connector labeled with "2"
 - 3) La marcatura va messa in corrispondenza del connettore GEISI contrassegnato con "3"
The marking must be set in correspondence of the GEISI connector labeled with "3"
 - 4) Colore giallo (Yellow)
 - 5) Colore nero (Black)
 - 6) Devono viaggiare accoppiati
Must travel coupled

REV	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99
COMP	WGER																																																																																																			
REVISION	130 A16-A24-A32 ALA F (Console)																																																																																																			
DATE	19.6.68																																																																																																			
BY	150 23 048																																																																																																			

GENERAL ELECTRIC
REVISIONS OF THE DESIGN

150 23 048

RIF. REF.	TIPO TYPE	MARCATURA CAVI CABLE LABELLING		FUNZ. FUNCT.	NOTE NOTES	RIF. REF.	KIT 1		KIT 2		DESCRIZIONE PARTI PARTS DESCRIPTION	KIT 1 COD. 0646767P		KIT 2		NOTE NOTES	
		LATO INT. ALL' U.F. SIDE INT. TO PH. UNIT	LATO EST. ALL' U.F. SIDE EXT. TO PH. UNIT				COD. CODICE CODE	Q	COD. CODICE CODE	Q		CODICE CODE	Q	CODICE CODE	Q		
												PEDANA BASE BULL.	0835988 K	2			
												PEDANA BASE	0835819 E	3			
												PEDANA - COPERCHIO PIATTO	0835821 D	4			
												PEDANA - COPERCHIO TAVOCCO TES.	0835823 M	1			
												COPERCHIO LATERALE LUNGA	0674390 T	2			
												PIASTRINA	0836464 B	4			
												VITE T.S. M4 x 20	5312748 E	1			
												VITE T.S. M5 x 25	5313729 B	10			
												VITE T.C. CAVA ESAG. M10x40	5313206 F	8			
												VITE T.S. CAVA ESAG. M10x50	5313208 G	8			
												RONDELLA PIANA ø 10,5	5331110 H	32			
												RONDELLA ELASTICA ø 10,5	5332110 S	16			
												DADO ESAG. MEDIO M10	5321110 M	16			
												BREAKER TQL 32010	0002114 E	1			
												VITE TS M4x8	6312743 Q	4			1

NOTE: 1) Vedi disegno (See dwg) n° 15043 905

NOTES:

REV 0 1 68 107 406 68
VEDI F.V. 21-3-68

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emiss.
appr. TR
Poppl.
I 51

LISTA CAVI E PARTI PER IL COLLEGAMENTO DI UNITA' FISICHE
CABLES AND PARTS LIST FOR PHYSICAL UNIT CONNECTION

GENERAL ELECTRIC

sez.-sec.
100

N° 150 23 0861
cont. su fo. 1

RIF. REF	TIPO TYPE	MARCATURA CAVI CABLE LABELLING		FUNZ. FUNCT.	NOTE NOTES	RIF. REF	KIT 1	KIT 2	DESCRIZIONE PARTI PARTS DESCRIPTION	KIT 1	KIT 2	NOTE NOTES
		LATO INT. ALL' U.F. SIDE INT. TO PH. UNIT	LATO EST. ALL' U.F. SIDE EXT. TO PH. UNIT				COD. 0646541 G	COD.		COD. 0646807 Q	COD.	
							CODICE CODE	Q		CODICE CODE	Q	
X	C13	AL117	ALA D ALI290 J1	T - CPU 1 - X	A.C.	1	C13 0540487H	1	BREAKER TOL 32015	0001356A	1	
				Y		2	C14 0640526D	1				
				Z		3	C15 0540517E	1				
				Gr		4	C16 0540611W	1				
				Cr		5	C17 0640528X	1				
X	C14	AL125	ALA D VAR300 P1-2	ALA F TAV460 P1-1	Contr.	6	C18 0540524K	1				
			3			2	C19 0640663B	1				
			4			5						
X	C15	AL141	ALA D VAR300 P1-9	ALA C VAR321 P20-7	Contr.	5						
			10			6						
			11			1						
X	C16	AL147	ALA D ALIO32 P2-14	ALA C VAR 321 P20-1	A.C.	2						
			15			3						
			13			1						
			17			5						
			16			4						
X	C17	AL125	ALA D VAR300 P1-1	ALA B VAR591 P1 -2	Contr.	6						
			2			6						
			4			5						
X	C18	AL141	ALA D VAR300 P1-9	ALA F VAR450 P1 -7	Contr.	5						
			10			6						
			11			1						
X	C19	AL147	ALA D ALIO32 P2-14	ALA F VAR450 P1-1	A.C.	2						
			15			3						
			13			1						
			17			5						
			16			4						

NOTE: 1) Colore NERO (BLACK) 2) Colore ROSSO (RED) 3) Colore BLU (BLUE)
 NOTES: 4) Colore VERDE (GREEN) 5) Colore MARRONE (BROWN) 6) Colore GIALLO (YELLOW)

X - PARTI MONTATE ALLA SPEDIZIONE
 X - PARTS ASSEMBLED WHEN DELIVERED

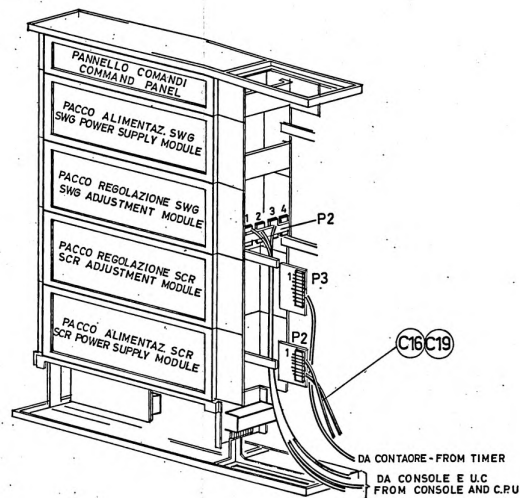
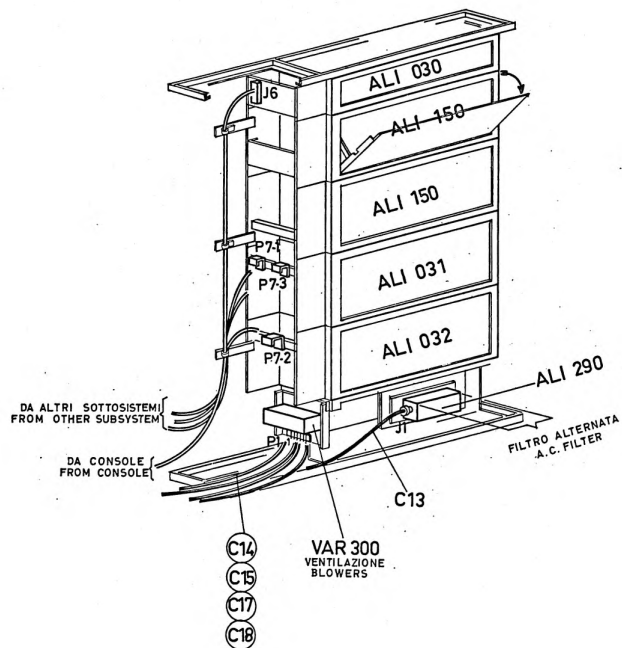
GENERAL ELECTRIC

sez.-sec. S.P.3
 loc. Premiana Milanese

N° 150 23 128 2
 cont.au.to. / to. 1

RIF REF	TIPO TYPE	MARCATURA CAVI CABLE LABELLING		FUNZ. FUNCT.	NOTE NOTES	RIF REF	KIT 1 COD. 0646543 Q		KIT 2 COD.		DESCRIZIONE PARTI PARTS DESCRIPTION	KIT 1 COD. 0646542 L		KIT 2 COD.		NOTE NOTES
		LATO INT. ALL' U.F. SIDE INT. TO PH. UNIT					LATO EST. ALL' U.F. SIDE EXT. TO PH. UNIT		CODICE CODE	Q		CODICE CODE	Q	CODICE CODE	Q	
		ATA C	P1				ATA D	ALI150 P2-								
X	C3	AL102	ATA C P1	ATA D ALI150 P2-	D.C.	1	C3	0640155H	4			GIUNZIONE ANELLI SUPERIORI	0674272 U	1		
X	C4	AL102	ATA C P1	ATA D ALI150 P2-2	D.C.	1	C4					GIUNZIONE PIEDI FINITO (A T)	0674268 M	1		
X	C5	AL101	ATA C P2	U-CPU- MASSA	D.C.	2	C7					COPERTITO GRIGLIATO GIUNZ. SUP.	0355830D	1		
X	C6	AL100	ATA C P3	ATA D ALI150 P2-3	D.C.	1	C8					FONDELLA GIUNZIONE PIEDI	0835835F	1		
X	C7	AL102	ATA C P4	U-CPU- +20	D.C.	1	C5	0640354 L	1			GRUPPO PANNELLO LATO CONSOLE	0355892Z	1		
X	C8	AL 102	ATA D P5	ATA D ALI150 P2-1	D.C.	1	C6	0640401 G	1			PANNELLO CAMINO CENTRALE	0674280Y	1		
												DISTANZILE PER GIUNZIONI	0355812Q	5		3
												VITE T.S. M4x12	6302735 G	2		
												PERNO PER ANELLO SUPERIORE	0835863 F	4		
												VITE T.C. CAVA ESAG. M10x50	6313200G	6		
												VITE T.C. CAVA ESAG. M10x60	6313210W	4		
												RONDELLA PIANA ø 10,5	6331110H	10		
												DADO ESAG. NORMALE M10	6321110M	6		
												RONDELLA ELASTICA ø 10,3	6332110S	10		
												PONT 2P	0618035V	2		
												PONT 2N	0618034Z	2		
												TAPPO C	0615232W	1		
												TAPPO DI CHIUSURA	0674263 R	1		
												RONDELLA PIANA ø 4.3	6331104 X	2		3
												DADO ESAGONALE M4	6321104 W	2		

MARCATURA CAVI CABLE LABELLING						FUNZ. NOTE		KIT 1				KIT 2				DESCRIZIONE PARTI PARTS DESCRIPTION		KIT 1		KIT 2		NOTE
RIF. REF	TIPÒ TYPE	LATO INT. ALL' U.F. SIDE INT. TO PH. UNIT	LATO EST. ALL' U.F. SIDE EXT. TO PH. UNIT	FUNCT.	NOTES	RIF. REF	COD. CODICE CODE	%	T	COD. CODICE CODE	Q					COD. CODICE CODE	Q	COD. CODICE CODE	Q		NOTES	
X	C1	AL141	ALI 260-1 P5-S	ALA PTA20/460 P1-7	Conti.	1	C1	0640545	F	1						Distanziale per giunzioni	0635512	Q	4			
			4			2	C3	0640543	G	2						Vite T.C. cava esar. M10X50	0313208	G	8			
			1			3	C4									Rondella piana Ø 10,5	0331110	H	16			
	C3	AL145	ALI 250-1 H		Ingresso rete	A.C.										Rondella elastica Ø 10,5	0332110	S	8			
	C4	AL145	ALI 260-2 H		Ingresso rete	A.C.										Dado M10	0321110	M	8			
																Coperchio grigliato	0635830	D	1			
																Fondello	0335835	F	1		4	
																Pannello	0674280	Y	1			
																Pannello camino centrale	0674282	D	1			
																Giunzione per anelli	0574272	U	1			
																Fermi per anelli	0635663	R	4			
																GIUNZIONE PIEDE	0674268	M	1			
NOTE: NOTES: 1 - Colore giallo - Yellow 2 - Colore nero - Black 3 - Colore marrone- Brown 4 - Vedi disegno (See dwg) n° 150 43 904																						
X Parti montate alla spedizione - Parts assembled when delivered.																						
VER. 0 GR 107 10-68 10-68 VERB. F.V.																						
COMP. Simboleni ALFA B9 Popol. AC POWER PANEL FOR BGS SYSTEMS												LISTA CAVI E PARTI PER IL COLLEGAMENTO DI UNITÀ FISICHE CABLES AND PARTS LIST FOR PHYSICAL UNIT CONNECTION 15023 5321 CONL. 44 10										
GENERAL ELECTRIC												S.P.S. Soc. Progamma Milano										



ALA D - WING D
ALIMENTAZIONE
POWER SUPPLY

GENERAL ELECTRIC		SCHEMA A BLOCCHI FISICO		MOD.	DATA	VISTO	N°. CODICE	
Scale	Firma	PHYSICAL BLOCK DIAGRAM		16/2/68	24/3/68	6/5/68	ngm	DISEGNO
ST		130A16-A24-A32		16/2/68	24/3/68	6/5/68		
MAT.	TT	FIN.					N°. DISEGNO 7-1(2) 150 43 008	

[illegible]

✱ PER L'IMPIEGO DEL TAV 421/c COLLEGARE IL CAVO (CX) A TAV 460-J1
 FOR USE TAV 421/c CONNECT (CX) CABLE TO TAV 460-J1

IL VAR 360/B È OPZIONABILE
 THE VAR 360/B IS OPTIONAL

VAR 360/B
 CONTAORE
 TIMER

VAR 360/B

VITE T.C. M4x10
 COD. 6311243 S

RONDELLA ELAST. Ø 4,3
 COD. 6332104 B

CON 460

DA ALIMENTATORE E DA
 ALTRI SOTTOSISTEMI
 FROM POWER SUPPLY AND
 OTHER SUBSYSTEM

VAR 380
 PROVA PIASTRE
 BOARD TESTER

CONSOLE OPERATIVA
 OPERATING CONSOLE

TAV 460

(CX) *

TAV 421/c
 TELECONSOLE
 REMOTE CONSOLE

CONSOLE DI MANUTENZIONE
 MAINTENANCE CONSOLE

CON 460
 MOBILE
 CABINET

(C2) + (C8)

VAR 450
 PANNELLO DISTRIBUZIONE
 ALTERNATE VENTILAZIONE
 BLOWER A.C. DISTRIBUTION
 PANEL

DA ALTRI SOTTOSISTEMI
 FROM OTHER SUBSYSTEM

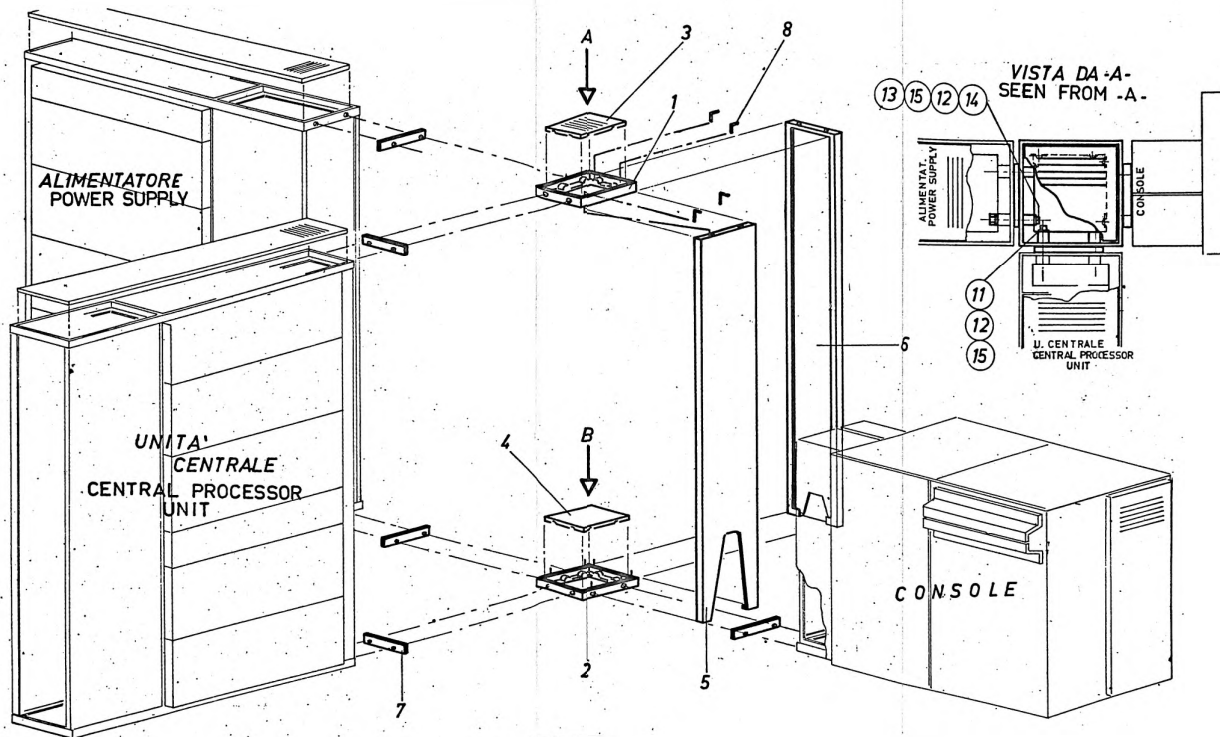
ALA F - WING F
 CONSOLE

GENERAL ELECTRIC		SCHEMA A BLOCCHI FISICO		MOD.	DATA	VISTO	N° CODICE
Scala	Firma LOCK	PHYSICAL BLOCK DIAGRAM		07/16	1-4-69	101	rpm
ST		130A16-A24-A32		SENZA 28-6-58			DISEGNO
MAT.		TT	FIN.	REP. 19-8-58	101		N° DISEGNO F.1(2)
				1-10-58			150 43 017

DA ALTRI SOTTOSISTEMI
 FROM OTHER SUBSYSTEM

[illegible]

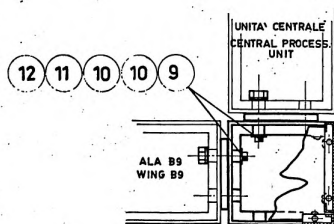
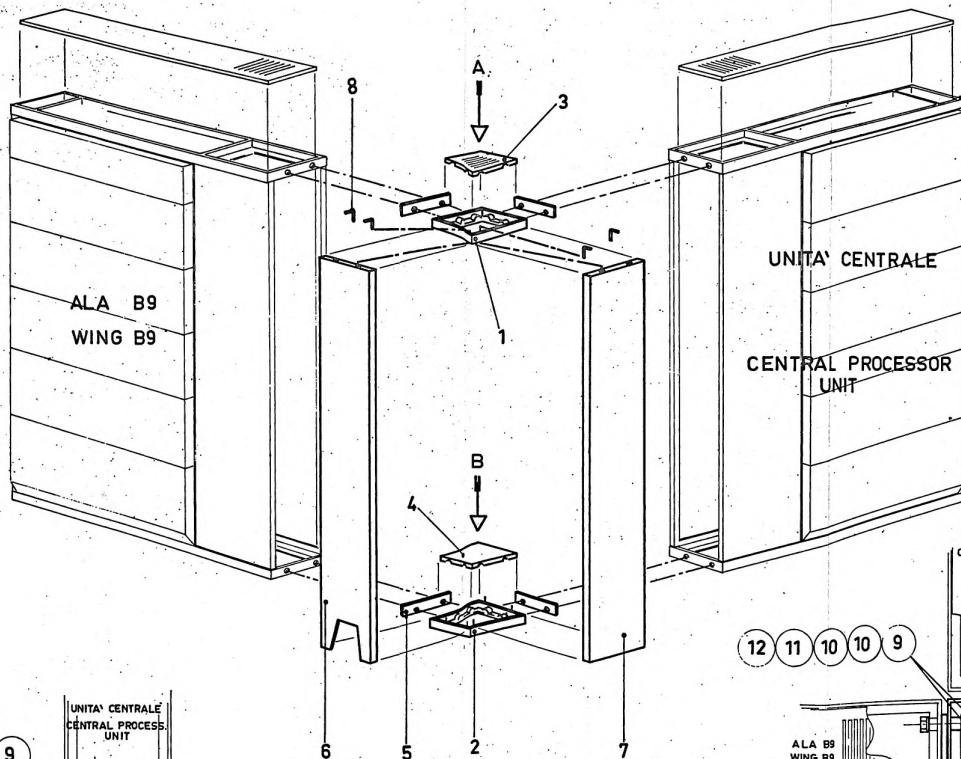
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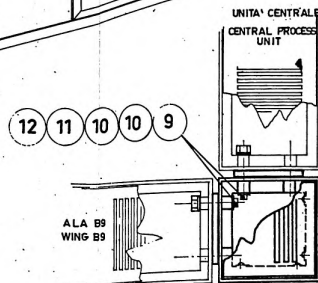
SU FOGLIO 2 SEGUE
DISTINTA MATERIALI
PARTS LIST FOLLOWS
ON SHEET 2

GENERAL ELECTRIC		COLLEGAMENTO U.E.		MOD.	DATA	VISTO	N. CODICE
Scale	Firma	PARTICOLARE 1		88P	29-5-68		npm
ST		PHYSICAL UNIT CONNECTION		943			DISEGNO
MAT.	TT	DETAIL No 1					N. DISEGNO 1/2
							15043900

[illegible]



VISTA DA-B- SEEN FROM-B-

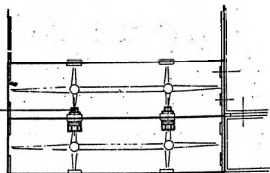


VISTA DA-A- SEEN FROM-A-

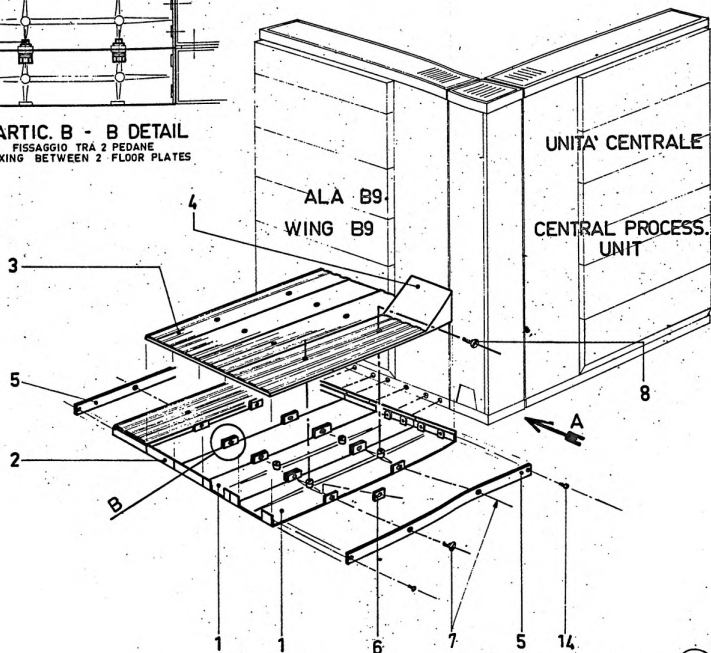
GENERAL ELECTRIC		COLLEGAMENTO U.F.		MOD.	DATA	VISTO	N°. CODICE
Scale	Firma	PARTICOLARE 5		68	10.6.68	10/3	rpm
ST	UTTERI	PHYSICAL UNIT CONNECTION					DISEGNO
MAT.	TT	DETAIL N° 5					N°. DISEGNO
							150 43 904

[illegible]

- 9
- 11
- 11
- 12
- 13



PARTIC. B - B DETAIL
FISSAGGIO TRA 2 PEDANE
FIXING BETWEEN 2 FLOOR PLATES



**VISTA DA -A-
SEEN FROM -A-
FISSAGGIO PEDANE AL PIEDE
FIXING OF FLOOR PLATE TO THE BASE**

- 13
- 12
- 11
- 11
- 10

SU FOGLIO 2 SEGUI
TABELLA MATERIALI
PARTS LIST FOLLOWS
ON SHEET 2

GENERAL ELECTRIC		COLLEGAMENTO U.F.		MOD.	DATA	VISTO	N° CODICE
Scale		Firma		68	10-1-68	RC	
ST		VIGER		107	27-9-68	RC	ngm
MAT.		TT		FIN.		DISEGNO	
						N° DISEGNO Fol (2)	
						150 43 905 1	

FIRMA SIGN	IND. ORIG.	GRUPPO-#GROUP IN 01 02 03 04 05 06	ORD.APPL.	REV.	O.TA	QTY. REQ. ATT. UL. ATT. UL. ATT. UL. ATT. UL. ATT. UL.										
10				VEN.F.V.	0	10 6 68	<div style="display: flex; justify-content: space-between;"> <div>QTY. REQ. ATT. UL. ATT. UL. ATT. UL. ATT. UL. ATT. UL. ATT. UL.</div> <div>QTY. REQ. ATT. UL. ATT. UL. ATT. UL. ATT. UL. ATT. UL. ATT. UL.</div> </div>									
10					1	27 9 68										
						QUANTITÀ: 01 02 03 04 05 06										
NUM.	INDOS.-DRAWING	N° COD.	DESCR.			01	02	03	04	05	06	UN	TD			
1	0835989K		PEDANA .BASE. BULL.													
2	0835819E		PEDANA .BAGN.													
3	0835821D		PEDANA .COPERCHIO PIATTO													
4	0835923M		PEDANA .COPERCHIO .IMBICO .TEST.													
5	0674330AT		COPERTURA .LATERALE .LUNGA													
6	0836464E		PIASTRINA													
7	6312749E		VITE .T.S. M4x20													
8	6313125B		VITE .T.S. M5x25													
9	6313206P		VITE .T.C. CAVA .ESAG. M10x40													
10	6313208G		VITE .T.C. CAVA .ESAG. M10x50													
11	6311101N		RONDELLA .PIANA .#10x5													
12	6332110S		RONDELLA .ELASTICA .#10x5													
13	6321101M		DADO .ESAG. MENO .M.10													
14	6312743B		VITE .T.S. M4x8													

RIF REF	TIPO TYPE	MARCATURA CAVI CABLE LABELLING		FUNZ. FUNCT.	NOTE NOTES	RIF REF	KIT 1 COD. 0646920		KIT 2 COD.		DESCRIZIONE PARTI PARTS DESCRIPTION	KIT 1 COD. 0646920W		KIT 2 COD. 0646924U		NOTE NOTES
		LATO INT. ALL' U.F. SIDE INT. TO PH. UNIT	LATO EST. ALL' U.F. SIDE EXT. TO PH. UNIT				CODE CODE	Q	CODE CODE	Q		CODE CODE	Q	CODE CODE	Q	
X	C1	AL 11	ALA E ALI290 J1	P-CPU2- Gf	A.C.	1	C1 0640487M	1			PANNELLO	0835978A	1	0835978A	1	
				Gf		2	C2 0640352T	1			DISTANZIALE PER GIUNZIONI	0835812Q	2	0835812Q	2	
				X		3	C3 0800646E	1			RONDELLA PIANA Ø 10,5	6331110N	4	6331110N	4	
				Y		4					DADO ESAGONALE NORMALE M10	6321110M	4	6321110M	4	
				Z		5					VITE T.O. CAVA ESAO. M10x50	631210W	4	631210W	4	9
X	C2	AL101	ALA E ALIO32 P7-2	ALA D ALIO32 P7-2	D.C.	3					RONDELLA ELASTICA Ø 10,3	6332110S	4	6332110S	4	
X	C3	DIF101	ALA E ALIO31 J3-1(1)	ALA D ALIO30 J4-3(1)		6					GIUNZIONE ANELLI SUPERIORE	0674272U	1	0674272U	1	
			J3-1(2)	J4-3(2)		6					GIUNZIONE ANELLI INFERIORE	0674268M	1	0674268M	1	
			J3-1(3)	J4-3(3)		6					PERNO PER ANELLO SUPERIORE	0835963R	2	0835963R	2	
			J3-1(4)	J4-3(4)		6										
			J3-1(5)	J4-3(5)		6										
			J3-1(6)	J4-3(6)		6										
			J3-2(1)	J4-4(1)		7										
			J3-2(2)	J4-4(2)		7										
			J3-2(3)	J4-4(3)		7										
			J3-2(4)	J4-4(4)		7										
			J3-2(5)	J4-4(5)		7										
			J3-2(6)	J4-4(6)		7										
			DA	A												
			J4-11(1)	J4-11(2)		8										
			J4-11(3)	J4-11(4)		8										

NOTE: 1 - VERDE (Green) - 2 - MARRONE (Brown) - 3 - NERO (Black) - 4 - ROSSO (Red)

NOTES: 5 - BLU (Blue) -

■ - IL NUMERO INDICATO TRA PARENTESI E' GIÀ FUNZIONATO SUI CAPPUCCI COPRI-FASTON

■ - THE NUMBER GIVEN IN PARENTHESES IS ALREADY WRITTEN ON THE FASTON COVERS.

6 - TERMINAZIONI CON CAPPUCCI COPRI-FASTON COLORE A 612 - (Terminals with faston covers color A612)

7 - TERMINAZIONI CON CAPPUCCI COPRI-FASTON COLORE A 604 - (Terminals with faston covers color A604)

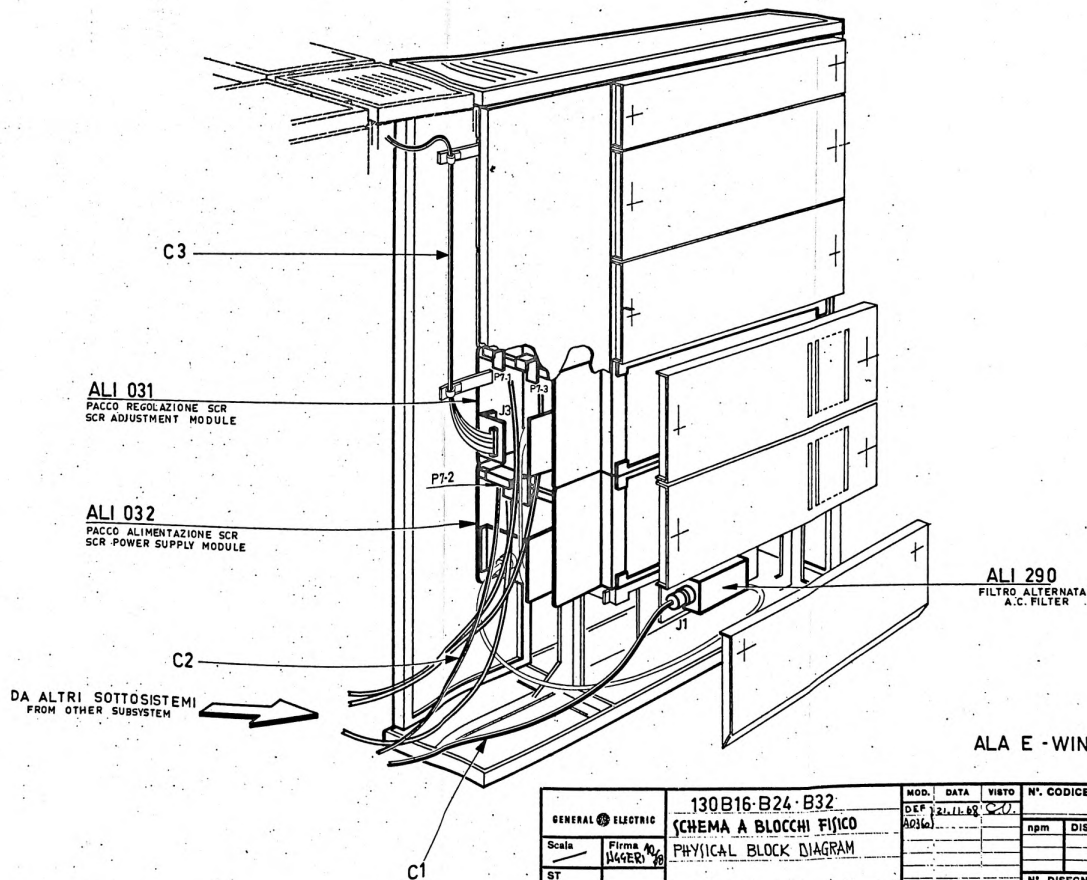
8 - TERMINAZIONI CON CAPPUCCI COPRI-FASTON COLORE A 643 - (Terminals with faston covers color A643)

X - PARTI MONTATE ALLA SPEDIZIONE (Parts assembled when delivered)

9 - KIT 1 - PER ASSEMBLARE VED. DISEGNI (for assemble see dwg.) 15043 913 - 15043 914

9 - KIT 2 - PER ASSEMBLARE VED. DISEGNI (for assemble see dwg.) 15043 913 - 15043 051

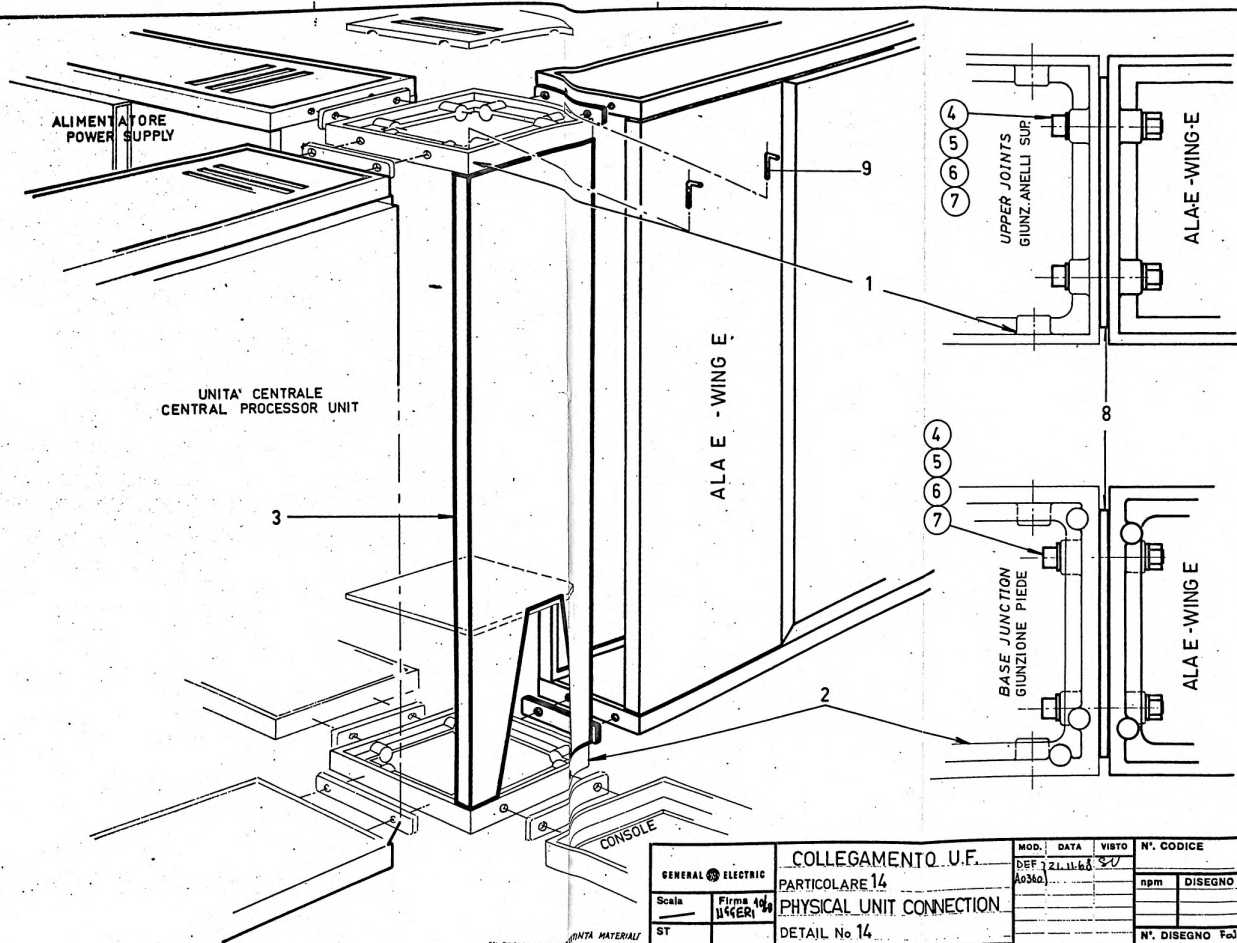
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comp. UGGERI emiss. appr. #post					
LISTA CAVI E PARTI PER IL COLLEGAMENTO DI UNITÀ FISICHE CABLES AND PARTS LIST FOR PHYSICAL UNIT CONNECTION 130 B16-B24-B32 AMPLIAMENTO ALIMENTATORE POWER SUPPLY EXTENDING					
GENERAL ELECTRIC sez. sec. fac. Tronina Milanese					
cont. su fo. 150 23 1360 to 1					



ALA E - WING E

GENERAL ELECTRIC		130B16-B24-B32		MOD.	DATA	VISTO	N° CODICE
SCHEMA A BLOCCHI FISICO		DEF 21.11.88		ADM		n°m DISEGNO	
PHYSICAL BLOCK DIAGRAM							
Scale	Firma M. BAGER						
ST							
MAT.	TT	FIN.				N° DISEGNO Fo.1(2)	
						15043 115	

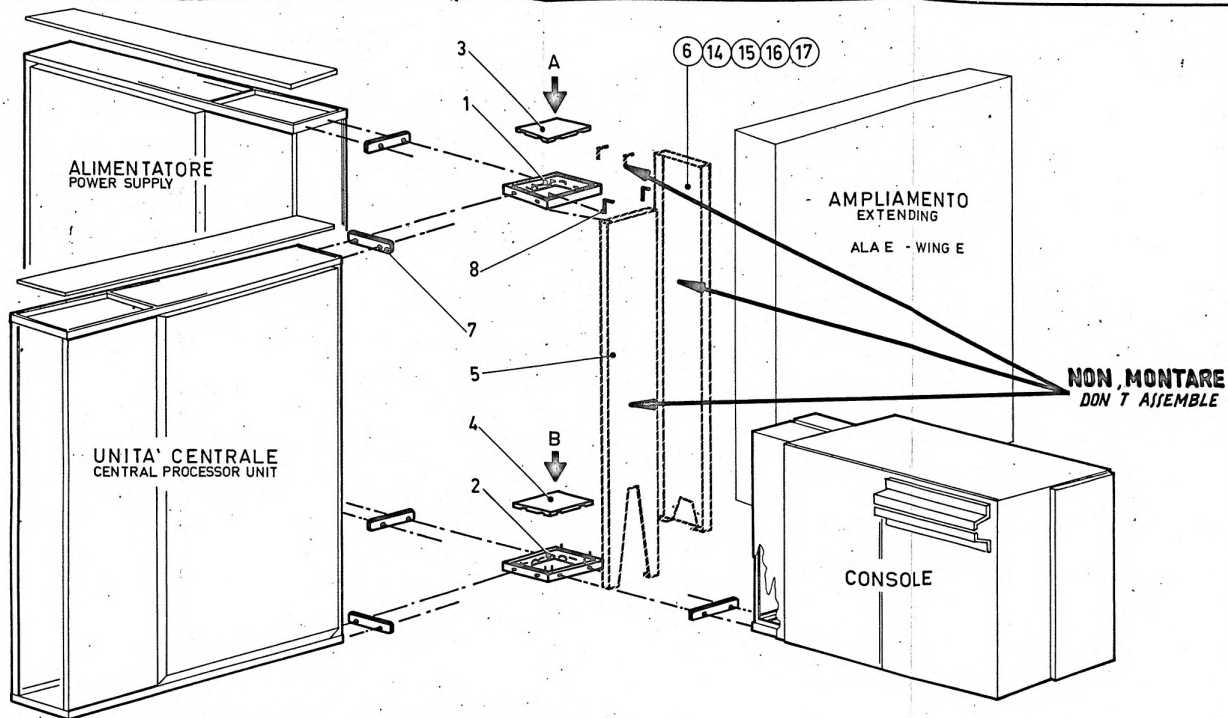
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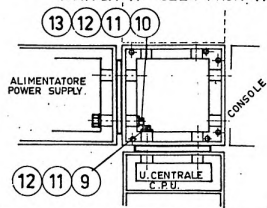
SU FOGLIO 2 SERVO IN SHEET 2
PART LIST FOLLOW

GENERAL ELECTRIC		COLLEGAMENTO U.F.		MOD.	DATA	VISTO	N. CODICE
Scale		PARTICOLARE 14		DEF	21.11.65	30	
ST		Firma 40					npm
MAT.		DETAL No 14					DISEGNO
							N. DISEGNO F01(2)
							150 43 913

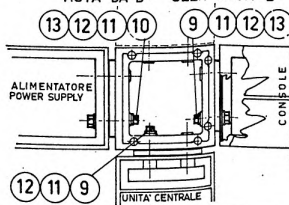
FIRMA SIVA	IND. ORIG.	GRUPPO-GROUP M. 01 02 03 04	ORD. APPL.	REV.	DATA	CON. REC.	ATT. UL	ATT. UL	ATT. UL	ATT. UL	ATT. UL	ATT. UL	ATT. UL	ATT. UL	ATT. UL
SV				048/AS3	21.11.58										
						QUANTITÀ 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000 1.000									
NO. ITEM	NPOS-DRAWING	NPCOD.	DESCR.			01	02	03	04	05	06	UM	TD		
1	0674272		GIUNZIONE ANELLI SUP.			/									
2	0674265		GIUNZIONE FIBRE FINIT.			/									
3	0835875		PANNELLO LATO. CAVALE.			/									
4	6312194		VITE F.C. CAVA. PSAG. M10x50			/									
5	6311114		BONDELLA PIANA M. 14x5			/									
6	6312114		BONDELLA ELASTICA M. 14x5			/									
7	6311114		DADO PSAG. M14			/									
8	0835812		DISTANZIALE PER GIUNZIONE			/									
9	08044.572	0835863	PERNO PER ANELLO SUP.			/									
TIT. COLLEGAMENTO U.F. PARTICOLARE 14															
PHYSICAL UNIT CONNECTION DETAIL No 14															
COMP.	048/AS3	10-5	STAND.	TP	FOR. N°	150 43 913									
APPROV.	[Signature]		GENERAL ELECTRIC			CONT. SU FO. 1 FO. 2									



VISTA DA -A- SEEN FROM -A-



VISTA DA -B- SEEN FROM -B-



IN FIGURA 2 SEGUE DISTINTA MATERIALI
PARTS LIST FOLLOWING ON SHEET 2

GENERAL ELECTRIC		COLLEGAMENTO U.F.		MOD.	DATA	VISTO	N° CODICE
Scala	Firma <i>U. KERN</i>	PARTICOLARE 15		DEF. 22.11.62	5-D		
ST		PHYSICAL UNIT CONNECTION					ngm DISEGNO
MAT.		DETAIL No 15					N° DISEGNO F. 1(2)
TT		FIN.					15043 914

[illegible]

GE 115/3 · 120 · 130

SOTTOSISTEMA UNITA' CENTRALE

CONSOLE—MPA—ALIMENTATORE—ALA B9

Catalogo parti di ricambio

SECONDA EDIZIONE

[illegible]**catalogo**

INDICE

GE 115/3 - 120 - 130 - SOTTOSISTEMA UNITA' CENTRALE

CONSOLE - MPA - ALIMENTATORE - ALA B9

Pag. 1

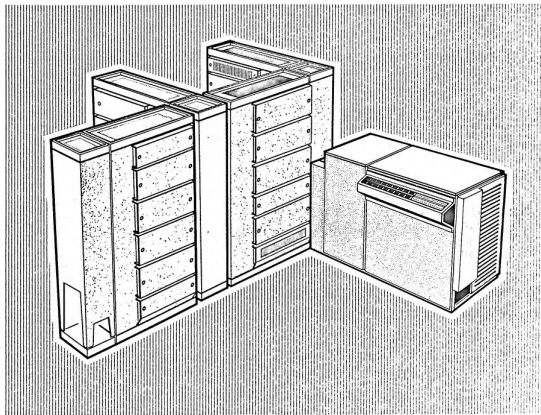
TAVOLA DI RIFERIMENTO	"	3
TAVOLA DI RIFERIMENTO	"	4
TAVOLA DI RIFERIMENTO	"	5
UNITA' CENTRALE TELAIO ELETTRONICA	"	6
UNITA' CENTRALE TELAIO ELETTRONICA (Figura)	"	7
UNITA' CENTRALE (MEM 470)	"	8
UNITA' CENTRALE (MEM 470) (Figura)	"	9
UNITA' CENTRALE PIEDE (VAR 321)	"	10
UNITA' CENTRALE PIEDE (VAR 321) (Figura)	"	11
UNITA' CENTRALE (COPERTURE)	"	12
UNITA' CENTRALE (COPERTURE) (Figura)	"	13
ALIMENTATORE SCR-ALA C (COPERTURE)	"	14
ALIMENTATORE SCR-ALA C (COPERTURE) (Figura)	"	15
ELENCO PIASTRINE	"	16
ELENCO PIASTRINE	"	17
ALIMENTATORE SCR (ALI 030 A/L)	"	18
ALIMENTATORE SCR (ALI 030 A/L) (Figura)	"	19
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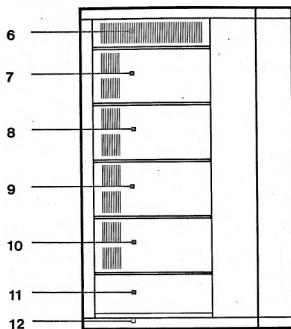
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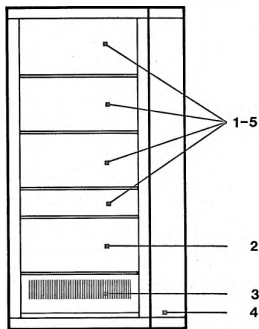
SOTTOSISTEMA UNITA' CENTRALE

CONSOLE - MPA - ALIMENTATORE - ALA B9



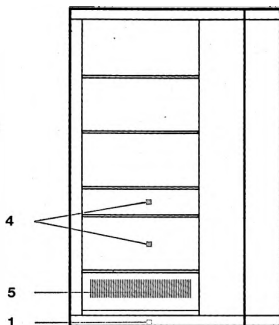


ALA D ALIMENTATORE

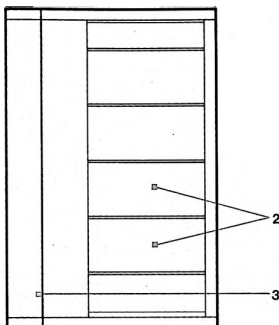


ALA C UNITA' CENTRALE

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2	Memoria (MEM 470)	8 - 9
3	Piede e VAR 321	10 - 11
4	Coperture - U.C. S.C.R.	12 + 15
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10	PST SETE-PIPA-CIBO-BOXENS. BOX AMP.	42 + 51
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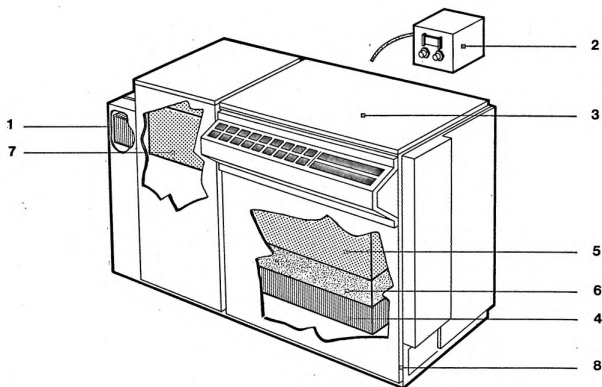


ALA M 64K



ALA B9

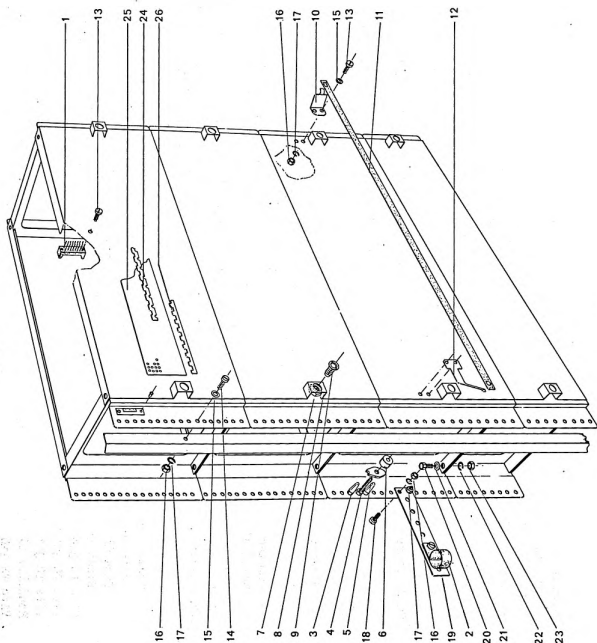
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1	Coperture ALA M	60 - 61
2	Alimentatore per altern. (ALI 260)	62 - 63
3	Coperture (ALA B9)	64 - 65
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5	Ventilatori (VAR 321)	10 - 11



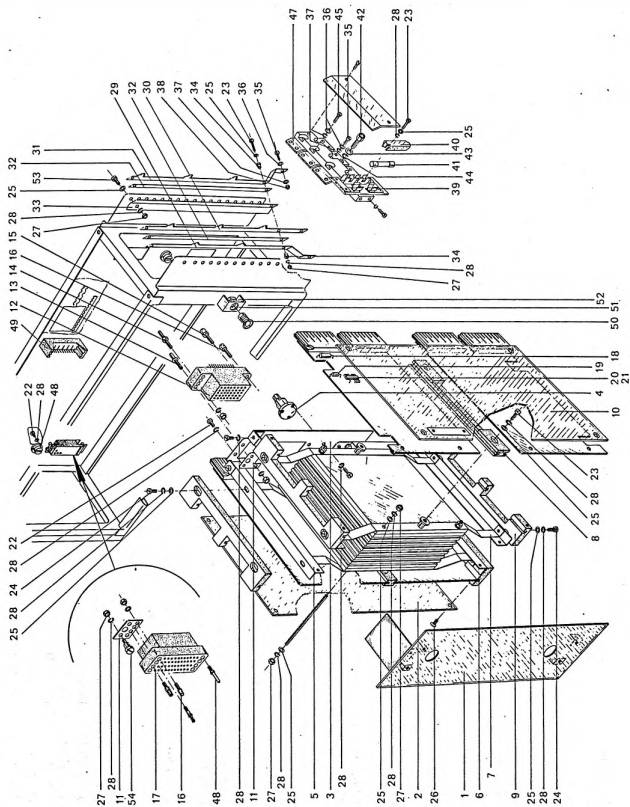
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1	Contaore (VAR 360)	66 - 67
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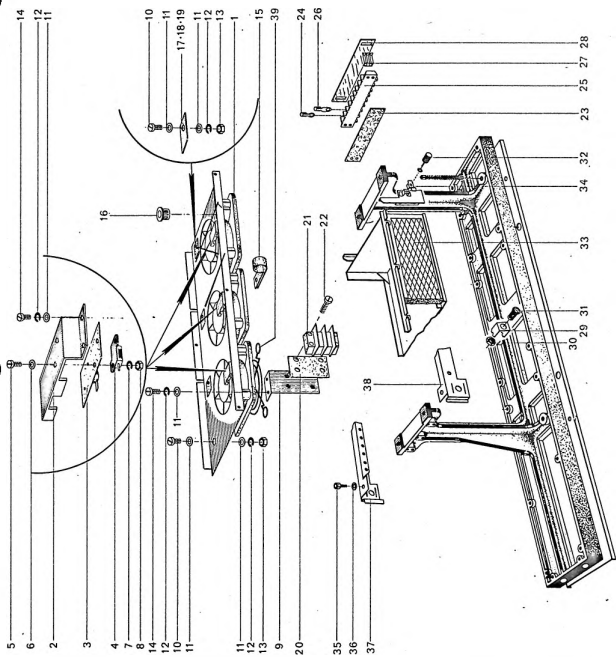
1	0834000 S	Connettore maschio
2	5618056 D	Serracavo Looping tipo 3
3	0839611 Q	Colonnina
4	0839609 V	Tirante
5	0839612 U	Premicavo
6	0839610 P	Pomello zigrinato
7	0835484 X	AG. Supporto fissaggio coperchio
7	0834662 U	Dado Fastener
8	0835132 C	Supporto
9	0834663 Y	Ricettacolo
10	0839473 S	Supporto a balestra destro
11	0839772 W	Riga numerata per pacchi
12	0839474 P	Supporto a balestra sinistro
13	6311231 R	Vite TC 3Max6
14	6311233 Z	Vite TC 3Max12
15	6331103 A	Rondella piana ø 3,2
16	6321103 H	Dado 3MA
17	6332103 N	Rondella elastica ø 3,2
18	6311232 V	Vite TC 3Max10
19	0834189 J	Bandella reggicavo
20	6313132 B	Vite TCE 5Max15
21	6331105 T	Rondella ø 5,3
22	6332105 F	Rondella elastica ø 5,3
23	6321105 S	Dado 5MA
24	0834009 V	Nastro isolante
25	0834007 C	Bandella di alimentazione
26	0834008 Z	Bandella di massa



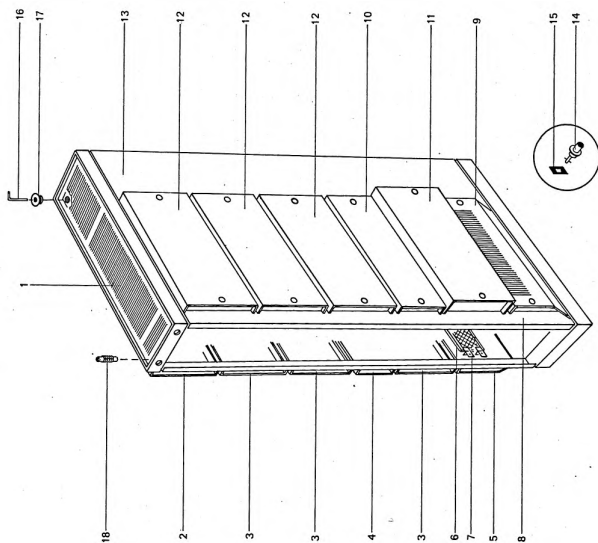
-	0646530 E	AG. Memoria	27	6321103 H	Dado M3
1	0842647 F	Assieme coperchio	28	6332103 N	Rondella elastica ϕ 3,2
2	0837733 B	Fiancata	-	0842598 F	AG. Barre di alimentazione
3	0837726 F	Piastra	29	0837673 D	Barra +12V
4	0837727 B	Spina	30	0837752 H	Barra di massa
5	0837729 U	Traversino vers. A	31	0837751 V	Barra +5V
6	0837728 Y	Traversino vers. B	32	0637754 S	Bandella isolante
7	0837735 U	Assieme traversino	33	0837749 W	Supporto barre
8	0837738 Z	Guida centrale	34	0837753 D	Boccola isolante
9	0837734 Y	Guida laterale	35	0680451 E	Vite TC 4x12
10	0842604 B	Assieme fiancata	36	0682456 X	Rondella piana ϕ 4,3
-	0842602 J	AP. Connettore maschio 75 CT	37	0683086 F	Rondella elastica ϕ 4,3
-	0842603 N	AP. Connettore femmina 75 CT	38	0682460 E	Dado M4
11	0837739 U	Piastrina fissaggio connettore	-	0842531 T	AG. Morsetteria tensioni
12	0001426 R	Bloccetto maschio 75 CT	39	0842590 G	Piastrina fusibile
13	0001699 R	Guida d'angolo maschio	40	0837670 U	Protezione fusibile
14	0001123 E	Maschio di accoppiamento	41	0001261 U	Fusibile 2A 250V
15	0001124 T	Femmina di accoppiamento	42	0680311 X	Vite TCE 8x15 ottone
16	0001700 K	Guida d'angolo femmina	43	0682560 L	Rondella piana ϕ 8,4 ottone
17	5617255 X	Bloccetto femmina 75 CT	44	0683131 E	Rondella elastica ϕ 8,4 B
-	0620227 Z	AP. Piastrina DIRE 2A (serie)	45	0680506 T	Vite TC 4x8 ottone
-	0620228 N	AP. Piastrina DIRE 2B (serie)	46	0837671 V	Traversino isolante
-	0620285 X	AP. Piastrina DIRE 2A (preserie)	47	0837742 G	Assieme piastrina
-	0620286 B	AP. Piastrina DIRE 2B (preserie)	48	0842755 S	Bussola con vite
18	5041050 Z	Cond. 1/0UF 3,5VL	49	0834000 S	Connettore maschio
19	4915012 W	Resistenza 12 K 0,1W	50	0834663 Y	Ricettacolo fastener
20	5829020 N	Pack diodi 8 DM (preserie)	51	0835132 C	Supporto
21	5823605 B	Diodo 1x9978 (serie)	52	0834662 U	Dado Fastener
22	6311230 Q	Vite TC 3x6	53	6311233 Z	Vite TC 3x12
23	6311234 N	Vite TC 3x15	54	0837741 U	Colonnina
24	6311232 V	Vite TC 3x10			
25	6331103 A	Rondella piana ϕ 3,2			
26	6312732 K	Vite TS 3x6			



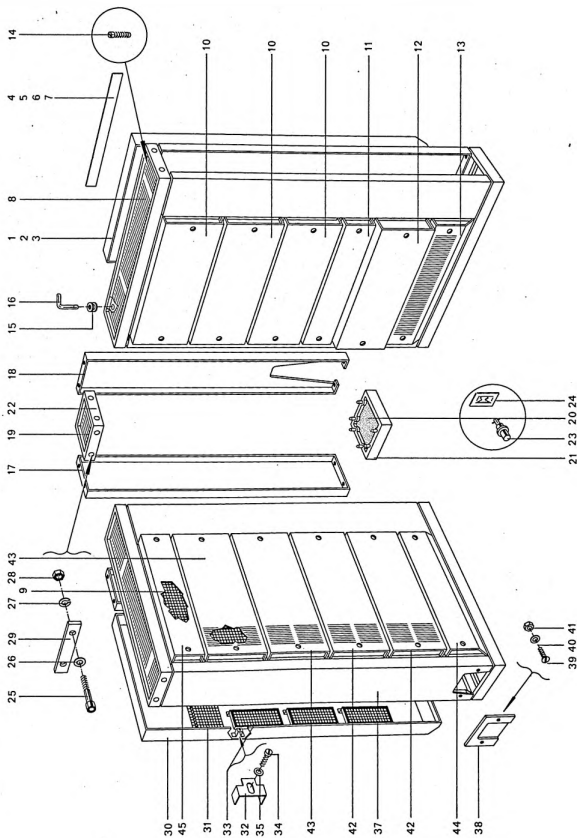
-	0646527 P	A3. Ventilatore			
1	0001614 C	Ventilatore Boxer 208-230-50-60 Hz			
-	0842609 G	AP. Protezione			
2	0837664 Z	Scatola			
3	0842638 T	Piastrina con termoswitch			
4	4962961 R	Resistenza 70Ω 8W			
5	6312725 F	Vite TS 2Max8			
6	7465700 P	Rondella piana ø 2,3			
7	0683542 T	Rondella elastica ø 2,3			
8	0682865 D	Dado 2MA			
9	0837409 G	Supporto morsettiere			
10	6311236 W	Vite TC 3Max20			
11	6331103 A	Rondella piana ø 3,2			
12	6332103 N	Rondella elastica ø 3,2			
13	6321103 H	Dado 3MA			
14	6311231 R	Vite TC 3Max8			
15	5618052 C	Serracavo Looping tipo 1			
16	0001876 F	Passacavo			
17	0831073 Z	Targhetta H1			
18	0831074 N	Targhetta H2			
19	0831075 J	Targhetta H3			
20	0001499 M	Piastrina numerata			
21	0001497 U	Morsettiere K502/A			
22	6311245 K	Vite TC M4x15			
23	5612989 D	Piastrina numerata			
24	5613350 W	Capocorda			
25	5612544 Q	Morsettiere K 609			
26	5613329 W	Capocorda			
27	0839653 U	Molletta tipo A			
28	0839360 E	Protezione morsettiere			
29	0835132 C	Supporto			
30	0834662 U	Dado Fastener			
31	0834663 X	Ricettacolo Fastener			
32	0837708 A	Vite bloccaggio filtro			
33	0001481 B	Filtro			
34	0837706 R	Squadretta bloccaggio filtro			
35	6311243 S	Vite TC M4x10			
36	6332104 B	Rondella elastica ø 4,3			
37	0674313 U	Angolare posteriore			
38	0674314 R	Angolare anteriore			
39	5541340 N	Origlia per ventilatore			



1	0835949 B	Coperchio grigliato superiore
2	0836280 Z	Copertura lato pins
3	0836268 N	Copertura lato pins
4	0836317 W	Copertura $\frac{1}{2}$ modulo
5	0835914 B	Coperchio piede grigliato
6	0001481 J	Filtro
7	0836291 T	Tassello fissaggio filtro
8	0835864 E	Canalotto piede
9	0835910 D	Coperchio piede grigliato
10	0835286 F	Copertura lato piastrine $\frac{1}{2}$ modulo
11	0674317 V	Coperchio memoria
12	0836264 N	Copertura lato piastrine
13	0835852 L	Pannello piede
14	0834661 Q	Pulsante CAMLOC
15	0834663 R	Staffa
16	0835863 R	Perno
17	9401020 E	Gommino
18	0835882 X	Perno per canallette



1	0674175 P	Coperchio lungo con scritta 130	31	0674128 P	Grigliato isolante
2	0674174 K	Coperchio lungo con scritta 115	32	0674127 S	Fermo per filtro
3	0674552 G	Coperchio lungo con scritta 120	33	0001482 W	Filtro
4	0819139 G	Targa U.C. 130	34	0836503 L	Vite speciale
5	0819140 E	Targa U.C. 120	35	6331104 X	Rondella piana ϕ 4,3
6	0819141 K	Targa U.C. 115			
7	0819142 K	Targa U.C. 105	36	0817045 W	Pannello piede
8	0817036 H	Coperchio grigliato sup.	37	0817081 W	Canaletta piede
9	0001481 J	Filtro per coperchio $\frac{1}{2}$ mod.	38	0817043 D	Tappo di chiusura
10	0836264 M	Coperchio 1M lato piastrine	39	6312735 G	Vite T.S. 4x12
11	0836286 F	Coperchio $\frac{1}{2}$ lato piastrine	40	6331104 X	Rondella piana ϕ 4,3
12	0674317 Y	Coperchio 1M lato memoria	41	6321104 W	Dado M4
13	0835910 D	Coperchio 1M per piede	42	0836507 M	Assieme coperchio
14	0835882 X	Perno filettato	43	0674183 F	Assieme coperchio
15	9401020 E	Gommone	44	0835943 R	Assieme coperchio piede
16	0835863 R	Perno per anello sup.	45	0836293 B	Assieme coperchio $\frac{1}{2}$ mod.
17	0817113 T	Pannello per camino			
18	0817490 G	Pannello per camino con finestra			
19	0817073 G	Coperchio grigliato per camino			
20	0835835 F	Fondello			
21	0674268 M	Giunzione piede			
22	0817083 R	Giunzione superiore			
23	0834661 Q	Pulsante			
24	0834665 R	Staffa elastica			
25	6313210 W	Vite TC CE 10x60			
26	6331110 N	Rondella piana ϕ 10,5			
27	6332110 S	Rondella elastica ϕ 10,5			
28	6321110 M	Dado M10			
29	0835812 Q	Distanziale			
-	0674124 N	AG. Copertura verticale alimentatore			
30	0674125 J	Coperchio verticale			



UCE 460 A/B

1	0610000 D	Piastrina ALAM 2A	31	0610031 V	Piastrina INTE 2B
2	0610002 J	Piastrina ANPL 2A	32	0610032 H	Piastrina INVE 2A
3	0610001 E	Piastrina ANDO 2A	33	0610033 D	Piastrina LIRI 2A
4	0610207 A	Piastrina CAIN 2A	34	0610081 A	Piastrina LIRI 2B
5	0610004 B	Piastrina CAIN 2B	35	0610082 N	Piastrina LIRI 2C
6	0610005 F	Piastrina CANA 2A	36	0610083 J	Piastrina LIRI 2E
7	0610006 K	Piastrina CANA 2B	37	0610084 F	Piastrina LIRI 2E
8	0610007 P	Piastrina CANA 2C	38	0610034 S	Piastrina LOBO 2A
9	0610008 C	Piastrina CISP 2A	39	0610035 W	Piastrina LOBO 2B
10	0610009 G	Piastrina COFA 2A	40	0610036 A	Piastrina LOOI 2A
11	0610010 S	Piastrina CONT 2A	41	0610037 E	Piastrina LOOI 2B
12	0610011 T	Piastrina COVE 2A	42	0610038 T	Piastrina LOOI 2C
13	0610012 F	Piastrina DECO 2A	43	0610039 X	Piastrina LOSE 2A
14	0610013 B	Piastrina DEEC 2A	44	0610040 V	Piastrina LOSE 2B
15	0610014 Y	Piastrina DEFO 2A	45	0610041 W	Piastrina LOSE 2C
16	0610015 U	Piastrina DEFO 2B	46	0610042 A	Piastrina LOSE 2D
17	0610016 G	Piastrina DERO 2A	47	0610043 E	Piastrina LOSE 2E
18	0610017 C	Piastrina DESA 2A	48	0610044 T	Piastrina LOSE 2G
19	0610018 Z	Piastrina DESA 2B	49	0610045 X	Piastrina LOSE 2H
20	0610019 V	Piastrina DESA 2C	50	0610046 B	Piastrina LOSE 2L
21	0610020 T	Piastrina DEVA 2A	51	0610047 F	Piastrina LOSE 2M
22	0610021 U	Piastrina ESCO 2A	52	0610051 X	Piastrina MAME 2A
23	0610022 G	Piastrina FIFA 2A	53	0610048 U	Piastrina NONA 2A
24	0610023 C	Piastrina FILC 2A	54	0610049 Y	Piastrina NORI 2A
25	0610025 V	Piastrina FILT 2B	55	0610050 W	Piastrina NORI 2A
26	0610026 H	Piastrina FILT 2C	56	0610052 B	Piastrina ORCA 2A
27	0610027 D	Piastrina GEMA 2A	57	0610053 F	Piastrina PATE 2A
28	0610028 S	Piastrina INFU 2A	58	0610054 U	Piastrina PINE 2A
29	0610029 W	Piastrina INIB 2A	59	0618035 V	Piastrina PONT 2P
30	0610030 U	Piastrina INTE 2A	60	0610057 G	Piastrina RECA 2A

UCE 460 A/B

61	0610058 V	Piastrina RECE 2A
62	0610059 Z	Piastrina REDI 2A
63	0610061 Y	Piastrina REGE 2A
64	0610060 X	Piastrina REGO 2A
65	0610062 C	Piastrina REGU 2A
66	0610063 G	Piastrina REIN 2A
67	0610064 V	Piastrina RENO 2A
68	0610065 Z	Piastrina REPO 2A
69	0610066 D	Piastrina RESI 2A
70	0610067 H	Piastrina RIIN 2A
71	0610068 W	Piastrina SEBO 2A
72	0610069 S	Piastrina STOL 2A
73	0610070 Y	Piastrina TEME 2A
74	0610071 Z	Piastrina TISE 2A
75	0610210 M	Piastrina TISE 2B
76	0610072 D	Piastrina TRIN 2A
77	0610073 H	Piastrina UARI 2A
78	0610074 W	Piastrina UARO 2A
79	0610075 S	Piastrina VARI 2A
80	0610055 Y	Piastrina VARI 2B
81	0610076 E	Piastrina VIAL 2A
82	0610213 W	Piastrina VORL 2A
83	0610214 K	Piastrina VIGI 2A
84	0610212 S	Piastrina VIMI 2A
85	0610215 P	Piastrina VINA 2A

UCE 462

86	0610002 J	Piastrina AMPL 2A
87	0618034 Z	Piastrina PONT 2N

UCE 463

88	0610002 J	Piastrina AMPL 2A
89	0610029 W	Piastrina INIB 2A
90	0610030 U	Piastrina INTE 2A
91	0618034 Z	Piastrina PONT 2N
92	0618035 V	Piastrina PONT 2P

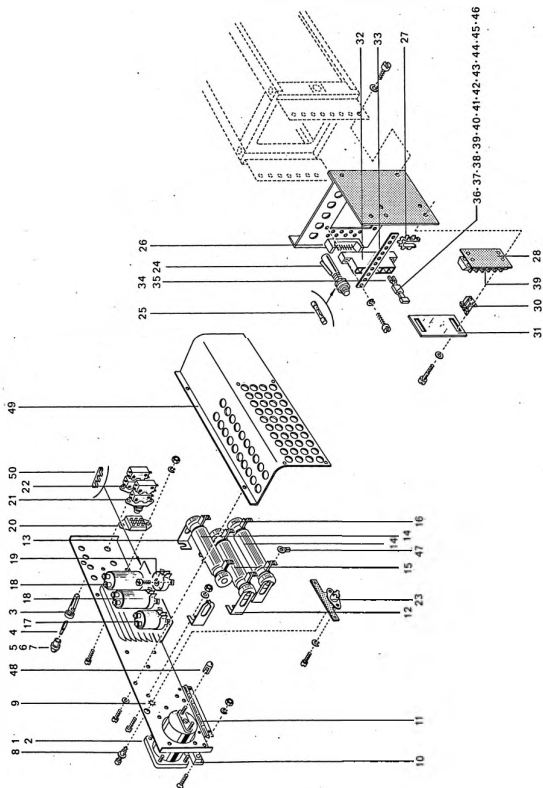
UCE 464

93	0610002 J	Piastrina AMPL 2A
94	0610029 W	Piastrina INIB 2A
95	0610030 U	Piastrina INTE 2A
96	0618034 Z	Piastrina PONT 2N
97	0618035 V	Piastrina PONT 2P

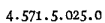
UCE 468

98	0610027 D	Piastrina GEMA 2A
99	0618034 Z	Piastrina PONT 2N
100	0618035 V	Piastrina PONT 2P

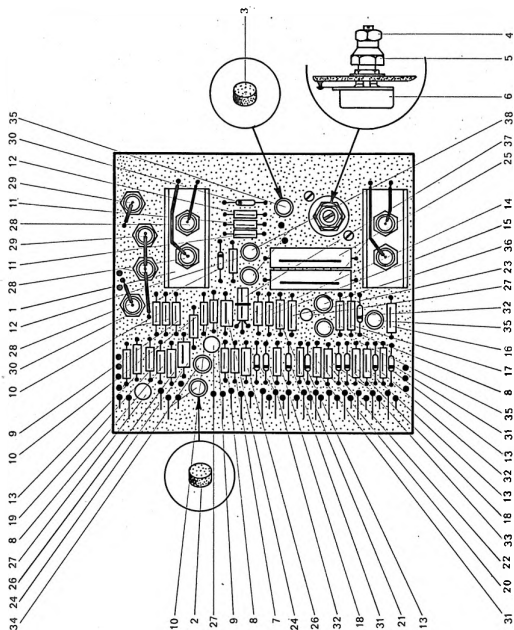
1	0000898 H	Contaore G.E.C. - 220V - 50 Hz	33	0839268 B	Barretta fissaggio connettori
2	0001317 A	Contaore G.E.C. - 240V - 60 Hz	34	0000883 J	Capocorda Faston
3	5363150 R	Portalamada	35	0001290 E	Capocorda Faston
4	5361011 M	Lampadino 12V	36	0830390 N	Cappuccio per terminale Faston - colore grigio scuro N° 1
5	5363152 W	Gemma rossa	37	0830391 P	Cappuccio per terminale Faston - colore grigio scuro N° 2
6	5363153 S	Gemma gialla	38	0830392 T	Cappuccio per terminale Faston - colore grigio scuro N° 3
7	5363154 P	Gemma verde	39	0830393 X	Cappuccio per terminale Faston - colore grigio scuro N° 4
8	1952133 X	Stelo con testa	40	0830394 L	Cappuccio per terminale Faston - colore grigio scuro N° 5
9	1952184 Z	Rondella dentata	41	0830395 Q	Cappuccio per terminale Faston - colore grigio scuro N° 6
10	0838686 G	Bloccchetto di fermo	42	0830396 U	Cappuccio per terminale Faston - colore grigio chiaro N° 1
11	0839101 R	Cerniera	43	0830397 Y	Cappuccio per terminale Faston - colore grigio chiaro N° 2
12	0001811 U	Supporto per resistori	44	0830398 M	Cappuccio per terminale Faston - colore grigio chiaro N° 3
13	4990060 X	Supporto per resistori	45	0830399 R	Cappuccio per terminale Faston - colore grigio chiaro N° 4
14	0001676 J	Resistenza 220 Ω 60W	46	0830400 T	Cappuccio per terminale Faston - colore grigio chiaro N° 5
15	0001674 A	Resistenza 64 Ω 60W	47	5613350 W	Capocorda AMP
16	0001805 G	Dischetti isolanti	48	0837285 B	Cappuccio isolante
17	0001307 L	Condensatore 1000 μ F 40V	49	0837180 T	Protezione resistenze
18	0001309 D	Condensatore 500 μ F 100V	50	5618320 N	Listello passacavo
19	0001402 S	Fascetta serracondensatori			
20	5104032 A	Deviatore a cursore			
21	5141204 J	Pulsante bipolare nero			
22	5141205 N	Pulsante bipolare rosso			
23	1952106 D	Ricettacolo CAMBLOC			
24	0001238 X	Portafusibile Littelfuse			
25	0001261 V	Fusibile 2A - 250V			
26	0834000 S	Connettore maschio Socapex			
27	0001858 W	Passacavo Weckesser			
28	0839086 H	Piastrina numerata			
29	5612540 D	Morsettiere Rhodex			
30	0839653 U	Molletta tipo A			
31	0839356 K	Protezione isolante per morsettiere			
32	0830388 L	Elemento per connettore Faston			



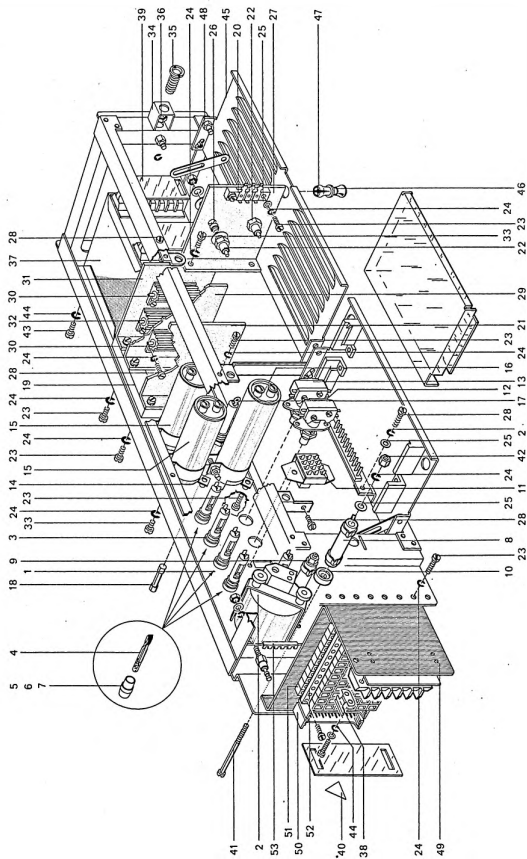
-	0835484 X	AG. Supporto fissaggio coperchio	31	0834229 E	Boccola
1	0835132 C	Supporto	32	0839097 E	Dissipatore
2	0834663 Y	Ricettacolo	33	0839100 Q	Dissipatore
3	0834662 U	Dado Fastener	34	0838961 G	Distanziatore
4	0001811 U	Supporto per resistori	35	0830388 L	Elemento per commettore Faston
5	0001987 N	Resistenza 47Ω 60W	36	0839089 W	Supporto connettore
6	0001805 G	Dischetto isolante	37	0830390 N	Cappuccio per terminale Faston - colore grigio scuro N° 1
7	0001985 E	Resistenza 100Ω 12W	38	0830391 P	Cappuccio per terminale Faston - colore grigio scuro N° 2
8	0001621 G	Resistenza 680Ω 15W	39	0830392 T	Cappuccio per terminale Faston - colore grigio scuro N° 3
9	0001807 Q	Resistenza 1Ω 25W	40	0830393 X	Cappuccio per terminale Faston - colore grigio scuro N° 4
10	0838685 U	Distanziatore	41	0830394 L	Cappuccio per terminale Faston - colore grigio scuro N° 5
11	0001605 V	Dischetto isolante	42	0830395 Q	Cappuccio per terminale Faston - colore grigio scuro N° 6
12	5613350 W	Capocorda AMP	43	0837134 L	Protezione piastrina PACO
13	5613333 D	Capocorda AMP			
14	5613520 F	Capocorda AMP			
15	0001810 T	Trasformatore T - 4000/22/5A			
16	0839653 U	Molletta tipo A			
17	0839357 P	Potenzionometro isolante			
18	0001370 W	Zoccolo Undecal			
19	0001296 L	Relé Ohmite			
20	0000883 J	Capocorda Faston			
21	4973076 A	Resistenza 100Ω 15W			
22	0001129 Y	Resistenza 120Ω 15W			
23	0001680 M	Resistenza 27Ω 15W			
24	4973471 U	Resistenza 270Ω 15W			
25	0002144 H	Resistenza 470Ω 15W			
26	0001858 W	Passacavo			
27	0838372 Q	Boccola isolante			
28	0001984 A	Diodo Zener			
29	5826513 A	Diodo Zener			
30	5826511 S	Diodo Zener 2L10			



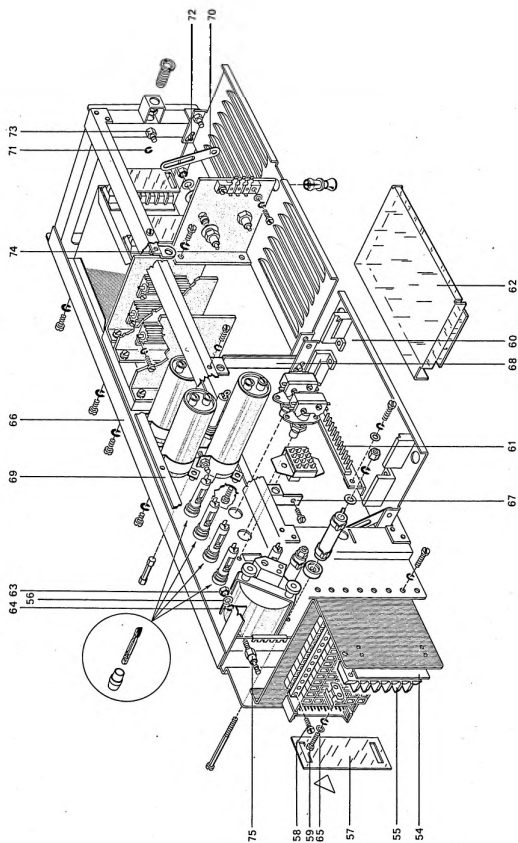
-	0620262 Y	AG. Piastrina PACO 03	32	5822468 S	Diodo
1	0838353 J	Dissipatore	33	5822725 X	Diodo
2	0839831 F	Distanziatore	34	5835860 A	Transistor
3	0839833 P	Distanziatore	35	5835750 N	Transistor
4	4999530 V	Dado per bloccaggio potenziometro	36	5831761 N	Transistor
5	4999550 X	Bussola per bloccaggio potenziometro	37	5831301 M	Transistor
6	4991522 F	Potenzimetro LESA	38	5835527 Z	Transistor
7	4933725 S	Resistenza 510 Ω			
8	4933607 J	Resistenza 390 Ω			
9	4934527 Y	Resistenza 3,3 K Ω			
10	4934327 P	Resistenza 2 K Ω			
11	4932525 S	Resistenza 33 Ω			
12	4934367 K	Resistenza 2,2 K Ω			
13	4923770 U	Resistenza 560 Ω			
14	4934446 X	Resistenza 2,7 K Ω			
15	4933202 D	Resistenza 150 Ω			
16	4924610 R	Resistenza 3,9 K Ω			
17	4924210 H	Resistenza 1,5 K Ω			
18	4924050 S	Resistenza 1 K Ω			
19	4923690 C	Resistenza 470 Ω			
20	4923610 V	Resistenza 390 Ω			
21	4924370 H	Resistenza 2,2 K Ω			
22	4924532 W	Resistenza 3,3 K Ω			
23	4923450 U	Resistenza 270 Ω			
24	5003395 L	Condensatore 0,1 μ F 63V			
25	5037955 Y	Condensatore 100 μ F 25V			
26	5031710 Z	Condensatore 47 μ F 6V			
27	5826600 E	Diodo Zener			
28	5824088 R	Diodo BYZ18			
29	5824032 X	Diodo BYZ12			
30	5826832 X	Diodo			
31	0001434 A	Diodo P100			



-	0842983	H	AG. Piastra	-	0832950	M	AP. Dissipatore
1	0836866	S	Piastra	28	6311230	Q	Vite TC 3x6
2	5254900	K	Portale	29	0836860	L	Dissipatore
3	5363150	R	Portalempada	30	4973750	X	Resist. 500Ω 50W
4	5361011	M	Lampada 12V	-	0842951	N	AP. Dissipatore
5	5363154	P	Gemma verde	31	0836859	N	Dissipatore
6	5363152	W	Gemma rossa	32	4973460	S	Resist. 250Ω 50W
7	5363153	S	Gemma gialla	33	6311231	R	Vite TC 3x8
8	4972756	H	Resist. 51Ω 15W	-	0835484	X	AG. Supporto coperchio
9	4973860	K	Resist. 680Ω 15W	34	0835132	C	Supporto
10	0001506	V	Rondella per resistenza	35	0834663	Y	Ricettacolo
11	5104032	A	Deviatore	36	0834662	U	Dado
12	5141200	L	Pulsante nero				
13	5141201	M	Pulsante rosso				
14	0838909	X	Fascetta cond.				
15	0001309	D	Cond. 500µF 100V	37	5445086	J	Trasformatore
16	5042437	L	Cond. 2600µF 50V	28	0839653	U	Molletta
17	0001238	X	Portafusibile	39	0839357	P	Protezione
18	0001259	V	Fusibile 1A 250V	40	3543104	P	Targhetta
-	0842948	W	AG. Dissipatori	41	6313113	D	Vite TC 3x55
19	0836863	V	Traversino	42	6321103	H	Dado M3
-	0842948	K	AP. Dissipatore	43	6311242	W	Vite TC 4x8
20	0836911	J	Assieme bloccetto	44	6332104	B	Rondella elastica ø 4,3
21	0836862	Z	Dissipatore	45	0836856	Z	Frontale
22	5826513	A	Coppia diodi	46	6380003	V	Pulsante
23	6311232	V	Vite TC 3x10	47	6380002	Z	Boccola
24	6332103	N	Rondella elastica ø 3,2	48	0839419	N	Perno inf.
25	6331103	A	Rondella piana ø 3,2	49	0842865	N	Supporto
26	0837265	M	Distanziatore	50	0834000	S	Connettore Socapex
-	0842949	P	AP. Dissipatore	51	0830388	L	Connettore Faston
27	0836861	M	Dissipatore	52	0839268	B	Barretta
				53	0001858	W	Listello passacavo



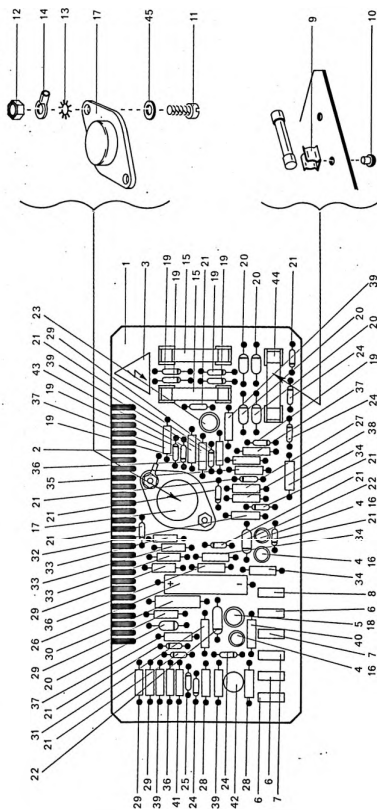
54	0836632 H	Piastrina isolante
55	5612540 D	Morsetti Rodex
56	7465702 U	Rondella piana ϕ 2,8
57	0839356 K	Piastrina isolante protezione
58	6311234 N	Vite TC 3x15
59	6311245 K	Vite TC 4x15
60	0836865 N	Frontale
61	0620143 Y	Piastrina COUN
62	0837160 R	Protezione
63	0682081 W	Dado 2,6 MA
64	0683545 Q	Rondella elastica ϕ 2,8
65	6331104 X	Rondella piana ϕ 4,3
66	0836405 B	Pacco $\frac{1}{2}$ mod.
67	0836857 V	Orecchietta
68	0836855 M	Traversino
69	0837263 V	Traversino
70	0837634 W	Guida mobile
71	6337106 Q	Anello di tenuta
72	0833359 N	Perno inferiore
73	0839418 J	Perno superiore
74	0836858 J	Squadretta
75	5613569 E	Torrette Gregorini



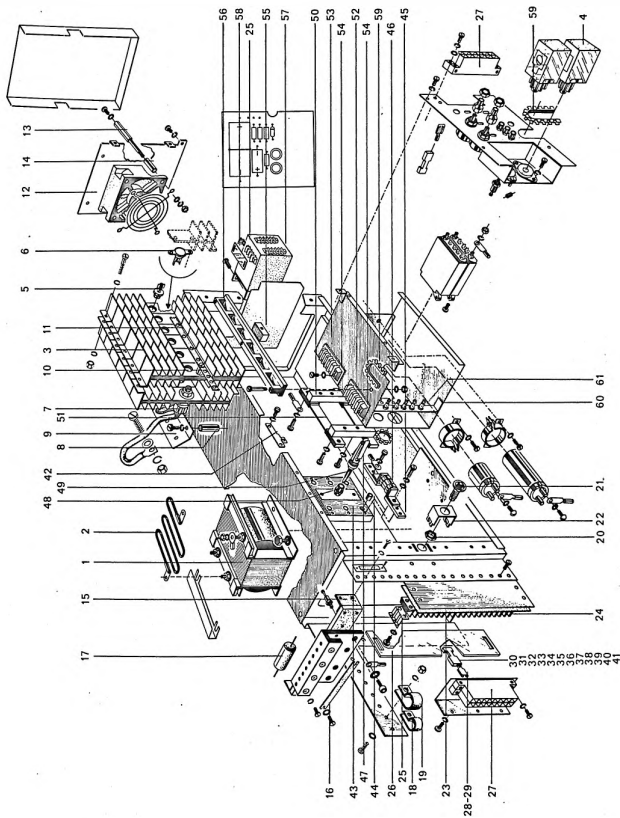
alimentatore SCR piastrina TESE (ALI 030/B)

GE 115/3 · 120 · 130 - catalogo

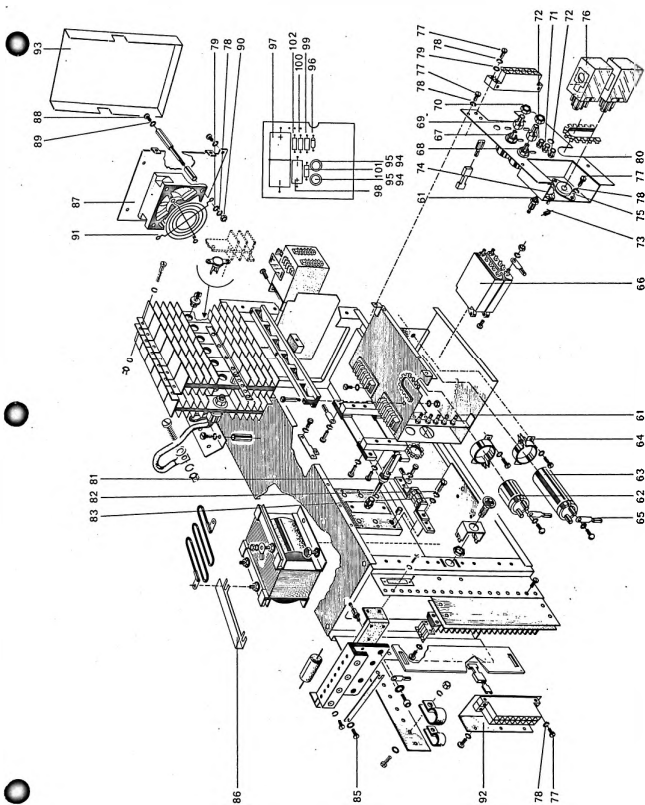
- 0620127 X	AG. Piastrina "TESE"		
1 0833819 M	Supporto stampato	32 4925610 M	Resist. 39 K. 0,25W
2 5617260 W	Terminali AMP	33 4934287 T	Resist. 1,8 K. 0,25W
3 3543104 P	Targhetta	34 4924050 J	Resist. 1 K. 0,25W
4 0839833 P	Distanziale	35 4925770 M	Resist. 56 K. 0,25W
5 0839831 F	Distanziale	36 4925050 N	Resist. 10 K. 0,25W
6 5610026 B	B. Sonda R.2. 582119.2	37 4924770 R	Resist. 5,6 K. 0,25W
7 5610028 U	B. Sonda R.2. 582119.9	38 4924370 H	Resist. 2,2 K. 0,25W
8 5610030 W	B. Sonda R.2. 582119.0	39 4923370 L	Resist. 220 Ω 0,25W
9 0000711 C	Portafusibile	40 4926050 S	Resist. 100 K. 0,25W
10 0000702 X	Rivetto	41 4923850 M	Resist. 680 Ω 0,25W
11 6311232 V	Vite 3x10	42 5884011 X	Circ. int. MA 711 C
12 6321103 H	Dado M3	43 5003395 L	Cond. 0,1 MF 63V
13 6332303 J	Rondella dentata ϕ 3,2	44 0001261 U	Fusibile 250W 2A
14 5613364 V	Capocorda	45 6331103 A	Rondella piana ϕ 3,2
15 0001259 V	Fusibile 250 V 1 A		
16 0000813 B	Trans. 1W 8918		
17 5836000 C	Trans. 2N 3772		
18 0000726 N	Trans. 1W 8916		
19 5822840 S	Diodo P400		
20 5826398 U	Diodo 398/B		
21 5822725 X	Diodo EB 1361		
22 5826842 Y	Diodo IZ C 12		
23 5814010 F	Diodo 2N 1596		
24 5824782 H	Diodo IS 2047/A		
25 5826022 D	Diodo IS 2056/A		
26 5038090 A	Cond. 250 MF 25V		
27 5031710 Z	Cond. 47 MF 6V		
28 5006776 T	Cond. 10 KpF 200V		
29 4933887 B	Resist. 750 Ω 5% 0,25W		
30 4964073 Z	Resist. 1 K. 5W		
31 4925130 D	Resist. 12 K. 0,25W		



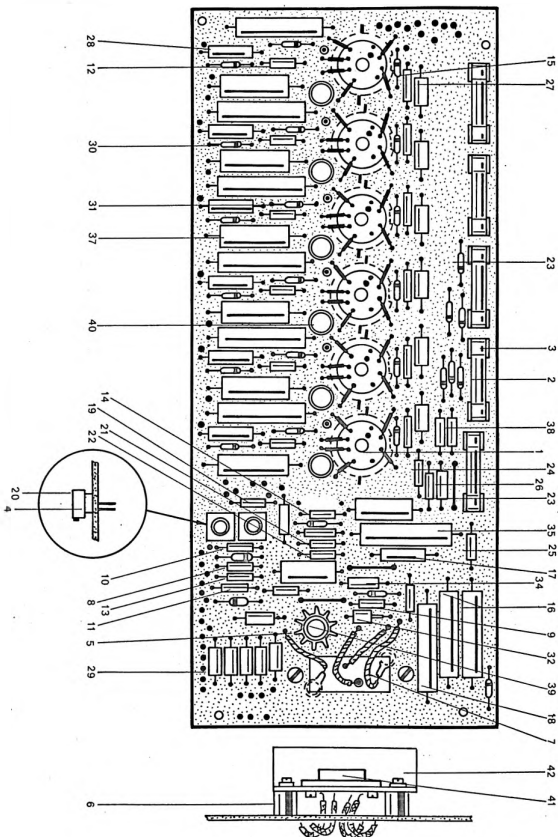
1	5421100 W	Bobina 3,5 mH/65V/L	30	0830390 N	Cappuccio colore grigio scuro N° 1
2	0842254 L	Resistenza 14 mΩ	31	0830391 P	Cappuccio colore grigio scuro N° 2
3	0839153 J	Dissipatore tipo A	32	0830392 T	Cappuccio colore grigio scuro N° 3
4	0001394 R	Relé Potter 115 V	33	0830393 X	Cappuccio colore grigio scuro N° 4
5	0842137 U	Diodo al silicio con dissipatore	34	0830394 L	Cappuccio colore grigio scuro N° 5
6	5241302 V	Termostato Texas	35	0830395 Q	Cappuccio colore grigio scuro N° 6
7	0001683 N	Diodo controllato Westinghouse	36	0830396 U	Cappuccio colore grigio chiaro N° 1
8	0839144 E	Bloccetto isolante tipo B	37	0830397 Y	Cappuccio colore grigio chiaro N° 2
9	0839143 R	Barra tipo A	38	0830398 M	Cappuccio colore grigio chiaro N° 3
10	0839147 J	Bloccetto isolante tipo C	39	0830399 R	Cappuccio colore grigio chiaro N° 4
11	0839158 G	Barra tipo B	40	0830400 T	Cappuccio colore grigio chiaro N° 5
12	0001316 E	Ventilatore Rotron	41	0830401 U	Cappuccio colore grigio chiaro N° 6
13	3838762 X	Distanziatore	42	0838752 W	Piastrina fissaggio circuito stampato
14	0838723 X	Distanziatore	43	0838756 X	Supporto fusibili
15	0842233 V	Morsettiere a due elementi	44	0001968 Z	Bussola ENSMT
16	0838387 W	Piastrina isolante	45	0838757 T	Piastrina fusibili
17	5038235 P	Condensatore elettrolitico 700 µF 25V/L	46	0001870 Z	Fusibili 150V 75A
18	5618054 V	Serracavo Looping tipo 2	47	5363150 R	Porta lampada RAFI
19	5618056 D	Serracavo Looping tipo 3	48	5363152 W	Gemma RAFI
			49	5361011 M	Lampada
20	0835484 X	AG. Supporto fissaggio coperchio	50	0839145 A	Bloccetto isolante tipo A
21	0834662 U	Dado Fastener	51	0000765 E	SHUNT INDEX 60 mV - 50A
22	0834663 Y	Ricettacolo	52	0838389 P	Piastrina con scritte P6
		Supporto	53	0838390 M	Piastrina con scritte P5
23	0839134 D	Piastrina con scritte	54	0000882 N	Morsettiere Rhodex
24	0001793 Z	Morsettiere Rhodex	55	0838759 L	Bloccetto
25	0839653 U	Molle tipo A	56	0838765 L	Supporto isolante dissipatori
26	0839368 D	Piastrina isolante	57	5455202 H	Trasformatore T4000/32/12
27	0830388 L	Elemento per connettore Faston	58	0839355 F	Piastrina isolante
28	0000883 J	Capocorda Faston	59	0001858 W	Passacavo Weckesser
29	0001292 E	Capocorda Faston	60	0838388 K	Squadretta fissaggio torrette
			61	5613369 E	Torretta Gregorini



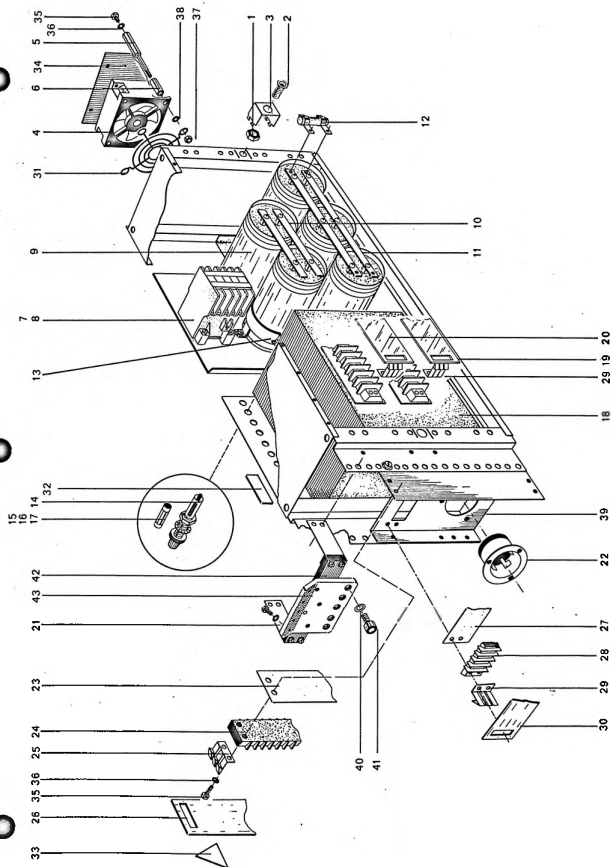
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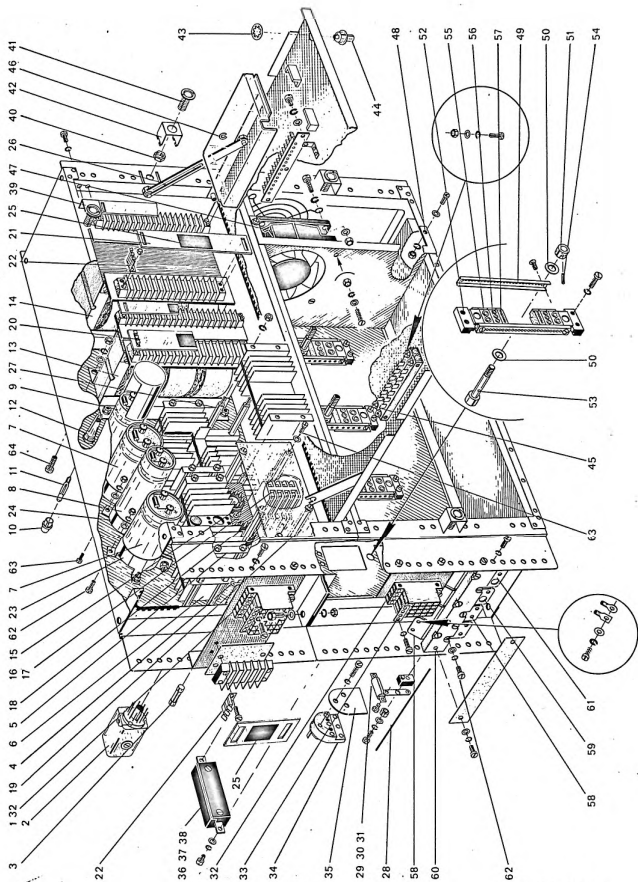
-	0620267	Y	AG. Piastrina OBLO 20	30	5822725	X	Diodo
1	0630609	A	Trasformatore d'impulso	31	5822468	S	Diodo
2	0001259	F	Fusibile 1A -250V	32	5822829	K	Diodo
3	0000711	N	Portafusibile	33	0001434	B	Diodo
4	0833831	F	Distanziatore	34	5041160	K	Condensatore 2,2 µF 35V
5	0001824	D	Missipiatore	35	5037955	V	Condensatore 100 µF 25V
6	0838383	V	Distanziale per dissipatore	36	5037781	J	Condensatore 50 µF 25V
7	5613347	E	Capocorda AMP	37	5003833	Q	Condensatore 1,6 µF 63V
8	4934327	P	Resistenza 2 KΩ	38	5006776	T	Condensatore 0,01 µF 200V
9	4933046	B	Resistenza 100Ω	39	0000726	N	Transistor
10	4933887	B	Resistenza 750Ω	40	5833575	V	Transistor
11	4934367	K	Resistenza 2,2 KΩ	41	5831018	K	Transistor
12	4933687	N	Resistenza 470Ω	42	0838382	Z	Dissipatore
13	4934086	G	Resistenza 1,1 KΩ - 0,5W				
14	4934047	U	Resistenza 1 KΩ (fino a matr. 0898)				
15	4923050	V	Resistenza 620Ω (da matr. 0899)				
16	4973846	X	Resistenza 100Ω				
17	0002121	A	Resistenza 680Ω 10W				
18	4973345	Q	Resistenza 680Ω 5W				
19	4934207	X	Resistenza 180Ω 10W				
20	0001728	Q	Resistenza 1,5 KΩ 2W (fino matr. 0898)				
21	4933846	T	Resistenza 1,1 KΩ (da matr. 0899)				
22	4934367	K	Potenzimetro 500Ω 0,5W				
23	4933527	E	Resistenza 680 KΩ 2W				
24	4934207	X	Resistenza 2,2 KΩ 2W				
25	4933725	S	Resistenza 330Ω 2W				
26	4964146	R	Resistenza 1,5 KΩ 2W				
27	4961840	G	Resistenza 50Ω 2W				
28	4962074	V	Resistenza 1,2 KΩ 3W				
29	4963071	U	Resistenza 6,8Ω 3W				
			Resistenza 10Ω 3W				
			Resistenza 100Ω 3W				



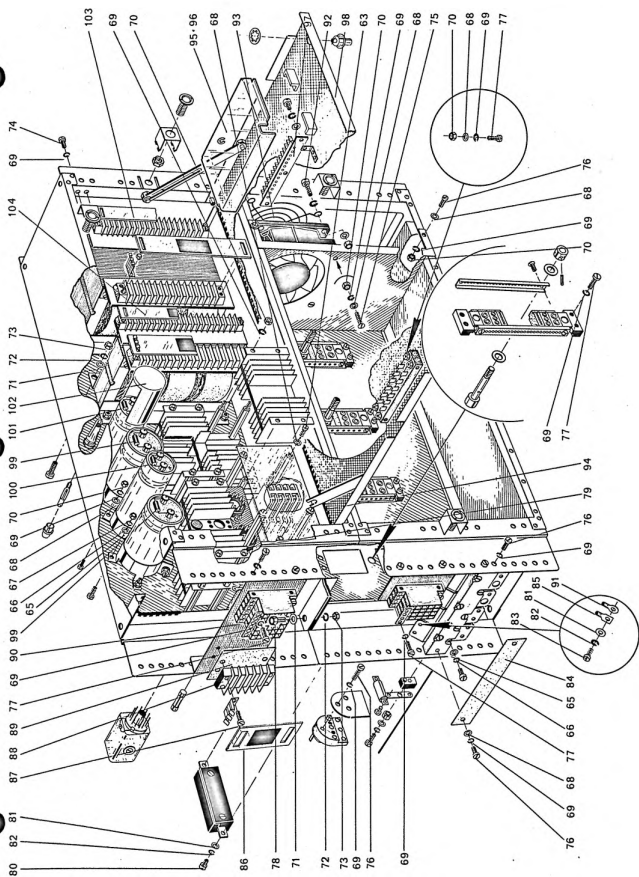
-	0835484 X	AG. Supporto fissaggio coperchio	31	5541340 N	Griglia per ventilatore
1	0834662 U	Dado Fastener	32	3543119 H	Targhetta
2	0834663 Y	Ricettacolo	33	3543105 K	Targhetta
3	0835132 C	Supporto	34	0838681 T	Piastra supporto ventilatore
4	0001316 E	Ventilatore Rotron 208/230 V - 50/60 Hz	35	0680341 S	Vite TC 4x10
5	0838762 X	Distanziatore	36	0683085 T	Rondella elastica ø 4,2
6	0838723 X	Distanziatore	37	0682868 A	Dado 3MA
7	5326226 X	Teleruttore Siemens 220V - 50 Hz	38	0683061 Q	Rondella piana ø 3,2
8	0001312 D	Teleruttore Siemens 208V - 60 Hz	39	0838772 Y	Supporto morsettiere.
9	0001682 S	Condensatore Sprague 44000 nF	40	0682560 L	Rondella piana ø 8,4
10	0839130 F	Barra corta	41	0680311 X	Vite TCCE 8x15
11	0839131 G	Barra lunga	42	0838750 R	Traversino isolante
12	0001129 Y	Resistenza SECI 120Ω 15W	43	0837693 P	Elemento di ancoraggio
13	5091062 A	Fascetta per condensatore			
14	0001238 X	Portafusibile			
15	0001252 F	Fusibile 8A.			
16	0001255 U	Fusibile 15A			
17	0001258 Z	Fusibile 0,5A			
18	5455200 V	Trasformatore trifase T4000/32/12			
19	0839379 A	Piastrina isolante			
20	0839382 V	Piastrina isolante			
21	0838720 N	Squadretta			
22	0001292 K	Spina Hubbel			
23	0839126 L	Piastrina con scritte			
24	0001793 Z	Morsettieria Rhodex			
25	0839653 U	Molletta tipo A			
26	0839368 D	Piastrina isolante			
27	0839129 H	Piastrina con scritte			
28	0001719 D	Morsettieria Rhodex			
29	0839652 Y	Molletta tipo B			
30	0839374 D	Piastrina isolante			



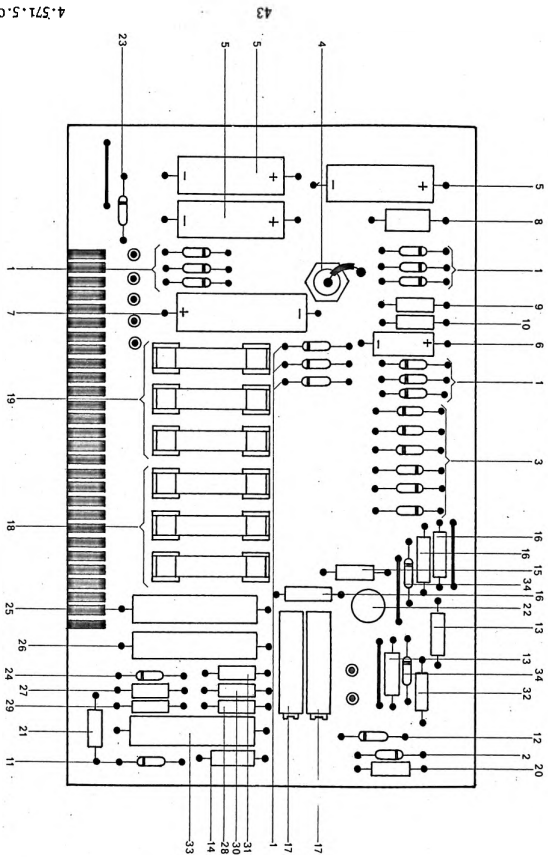
1	0001386 M	Relé Potter 12 V	33	0839263 M	Barretta di fissaggio elementi
2	0001394 E	Relé Potter 115 V - 50/60 Hz	34	0842616 G	Sezionatore
3	0001250 S	Fusibile 3A 250V	35	0837678 T	Piastrina numerata per sezionatore
4	0001238 X	Portafusibile Litteckfuse	36	5268052 Z	Derivatore 10A - 60 mV Index
5	0842781 C	Dissipatore con diodi	37	5268054 J	Derivatore 6A - 60 mV Index
6	0842780 B	Dissipatore con diodi	38	5268060 M	Derivatore 2A - 60 mV Index
7	0001324 X	Condensatore 11000 µF 25V _L	39	0839420 L	Squadretta
8	5038080 C	Condensatore 6000 µF 25V _L	40	0834662 U	Dado
9	5042437 L	Condensatore 2600 µF 50V _L	41	0834663 Y	Boccola
10	5363152 W	Gemma rossa RAFI	42	0835484 X	Supporto
11	5361011 M	Lampada 12 V	43	0834665 R	Staffa
12	5363150 R	Porta lampada RAFI	44	0834661 Q	Pulsante
13	5455224 Q	Trasformatore tipo T 4000/32/21	45	0830388 L	Elemento per terminali Faston
14	5455222 X	Trasformatore tipo T 4000/32/20	46	6337106 Q	Anello elastico
15	0001663 L	Zoccolo octal	47	0001614 C	Ventilatore Rotron 220V - 50/60 Hz
16	5326640 T	Teleruttore 50 Hz	48	0837943 Z	Supporto ventilatore
17	0001847 G	Teleruttore 60 Hz	49	0830512 X	Rotaia
18	0837988 T	Distanziatore	50	6331108 Y	Rondella piana ø 8,4
19	0837143 Y	Protezione teleruttore	51	0837933 Y	Manicotto
20	0839367 Q	Protezione morsetti	52	5616415 B	Squadra con guida
21	0839366 L	Protezione morsetti	53	0837924 M	Vite di bloccaggio connettore
22	0839653 U	Molletta tipo A	54	6343080 G	Spina elastica 2x12
23	0002138 H	Fascetta tipo 1262 Z	55	5616459 G	Elemento femmina 25A
24	0001402 S	Fascetta tipo 1420 Z	56	5616457 P	Elemento femmina 15A
25	0831766 S	Targhetta	57	5616455 F	Elemento femmina 5A
26	0839421 M	Guida mobile	58	0837743 C	Piastrina morsetto
27	0838137 M	Distanziale	59	0837742 G	Piastrina morsetto
28	0837679 K	Supporto fusibili	60	0837748 S	Traversino isolante
29	5373104 X	Fusibile 15A 450V extrarapido	61	0837926 U	Piastrina morsetto
30	5373102 D	Fusibile 10A 450V extrarapido	62	6311244 P	Vite TC 4x12
31	5373100 Z	Fusibile 5A 450 V extrarapido	63	6311232 Y	Vite TC 3x10
32	0830388 L	Elemento Faston	64	6311256 Y	Vite TC 5x10



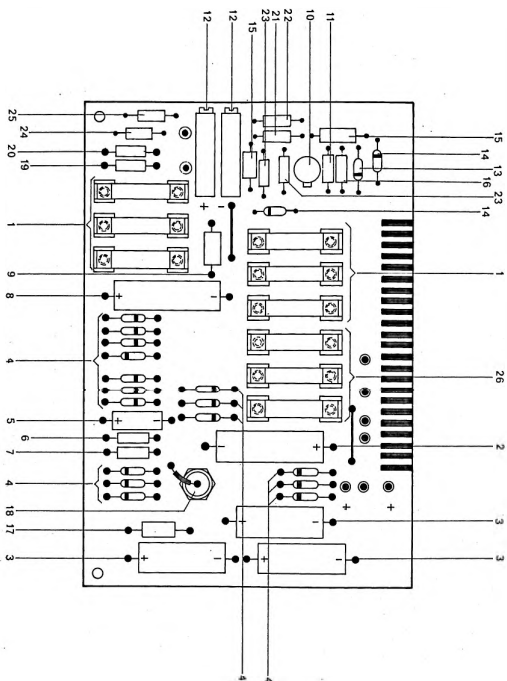
65	6331104 X	Rondella piana ø 4,2	97	0620233 Z	Piastrina COSE
66	6332104 B	Rondella elastica ø 4,2	98	0842514 W	Assieme frontale
67	6321104 W	Dado M4	99	4934367 K	Resistenza 2,2 K Ω $\frac{1}{4}$ W 2%
68	6331103 A	Rondella piana ø 3,2	100	4934527 T	Resistenza 3,3 K Ω $\frac{1}{4}$ W 2%
69	6332103 N	Rondella elastica ø 3,2	101	4934926 Q	Resistenza 8,2 K Ω $\frac{1}{4}$ W 2%
70	6321103 H	Dado M3	102	0837218 M	Cappuccio isolante
71	6331105 T	Rondella piana ø 5,3	103	0839352 J	Protezione Morsettiera
72	6332105 F	Rondella elastica ø 5,3	104	0839353 N	Protezione morsettiera
73	6321105 S	Dado M5			
74	6311230 Q	Vite TC 3x6			
75	6312736 L	Vite TS M3x15			
76	6311231 R	Vite TC M3x8			
77	6311234 N	Vite TC M3x15			
78	6313132 B	Vite TCCE M5x15			
79	0001370 W	Zoccolo Undecal			
80	0680490 Q	Vite TC M4x6			
81	0682456 X	Rondella piana ø 4,3			
82	0683086 F	Rondella dentellata ø 4,3			
83	0680506 T	Vite TC M4x8			
84	0837893 C	Targhetta			
85	5613333 D	Capocorda AMP			
86	0839356 K	Protezione morsettiera			
87	6311245 K	Vite TC M4x15			
88	5612540 D	Morsettiera			
89	0837969 M	Piastrina numerata			
90	0839265 E	Barretta di fissaggio elementi			
91	5613350 W	Capocorda AMP			
92	6311236 W	Vite TC 3x20			
93	5441340 N	Griglia ventilatore			
94	5618320 N	Listello passacavo			
95	0837173 T	Protezione piastrina PIPA A/B			
96	0837172 X	Protezione piastrina SETE A			



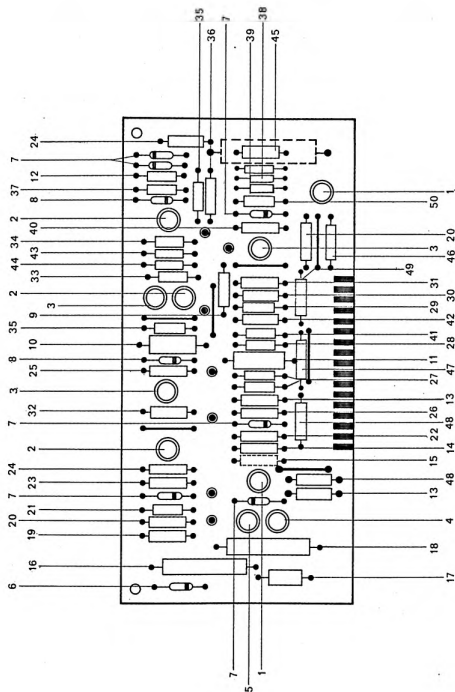
-	0620236 V	AG. Piastrina SETE A - 20 V	
1	0001434 A	Diodo P100	32 4933486 N
2	5822725 X	Diodo EB1361	33 4973660 W
3	5826398 U	Diodo 398 B	34 5824782 H
4	5826845 M	Diodo Zener 2x16	
5	5035210 Q	Condensatore 500 μ F - 16 VL	Resistenza 300 Ω - 2% (per SETE A)
6	5041560 T	Condensatore 22 μ F - 35 VL	Resistenza 390 Ω - 2% (per SETE A)
7	0001501 Q	Condensatore 100 μ F - 50 VL	Diodo Zener 1S 2047/A
8	4961791 T	Resistenza 5,6 Ω - 3 W	
9	4933687 N	Resistenza 470 Ω - 0,5 W	
10	4933127 W	Resistenza 120 Ω - 0,5 W	
11	5826022 B	Diodo Zener 1S 2056/A	
12	5826842 Y	Diodo Zener 12 C12 T	
13	5006776 T	Condensatore 10 KpF 200 V	
14	5037500 R	Condensatore 15 μ F 20 V	
15	4933329 S	Resistenza 200 Ω 2%	
16	4923370 L	Resistenza 220 Ω	
17	4991300 Y	Potenziometro 500 Ω - Trimit	
18	0001257 C	Fusibile 0,25 A - 250 V	
19	0001258 Z	Fusibile 0,5 A - 250 V	
20	4934047 U	Resistenza 1 K Ω - 2%	
21	4934446 X	Resistenza 2,7 K Ω - 2%	
22	584011 X	Circuito integrato μ A - 711 C	
23	0001434 A	Diodo P100 (per SETE A)	
24	5822725 X	Diodo EB1361 (per SETE A)	
25	4973845 U	Resistenza 180 Ω - 10 W (per SETE A)	
26	4975846 X	Resistenza 680 Ω - 10 W (per SETE A)	
27	4934247 P	Resistenza 1,6 K Ω - 2% (per SETE A)	
28	4933926 T	Resistenza 820 Ω - 2% (per SETE A)	
29	4934247 P	Resistenza 1,6 K Ω - 2% (per SETE A)	
30	4933846 T	Resistenza 680 Ω - 2% (per SETE A)	
31	4933405 E	Resistenza 240 Ω - 2% (per SETE A)	



-	0620239 K	AG. Piastrina A + 5 V			
-	0620238 P	AG. Piastrina B + 12 V			
1	0001257 C	Fusibili 0,025 A		25 { 4932925 K	Resistenza 82 Ω 2% per PIPA A
2	0001501 Q	Condensatore 100 μ F - 50 VL		25 { 4933127 W	Resistenza 120 Ω 2% per PIPA B
3	5035210 Q	Condensatore 500 μ F - 16 VL		26 0001258 Z	Fusibile 0,5 A - 250 V
4	0001434 A	Diodo P100			
5	5041560 Q	Condensatore 22 μ F - 35 VL			
6	4931127 W	Resistenza 120 Ω - 0,5 W			
7	4933687 N	Resistenza 470 Ω - 0,5 W			
8	5038090 A	Condensatore 250 μ F - 25 VL			
9	4964071 R	Resistenza 1 K Ω - 3 W			
10	5884011 X	Circuito integrato μ A 711 C			
11	4923370 L	Resistenza 220 Ω			
12	4991300 Y	Potenzimetro 500 Ω - Trimit			
13	5822725 X	Diodo EB 1361			
14	5824782 H	Diodo Zener 1S 2047 A			
15	5006776 J	Condensatore 10 KpF 200 V			
16	5037500 R	Condensatore 15 μ F 20 VL			
17	4961791 T	Resistenza 5,6 Ω 3 W			
18	5826845 M	Diodo Zener Zx16			
19	{ 4933645 S	Resistenza 430 Ω 2% per PIPA A			
	{ 4934047 U	Resistenza 1 K Ω 2% per PIPA B			
20	{ 4933645 S	Resistenza 430 K Ω 2% per PIPA A			
	{ 4934125 B	Resistenza 1,2 K Ω 2% per PIPA B			
21	{ 4934047 U	Resistenza 1 K Ω 2% per PIPA A			
	{ 4933967 T	Resistenza 910 Ω 2% per PIPA B			
22	{ 4933926 T	Resistenza 820 Ω 2% per PIPA A			
	{ 4933967 T	Resistenza 910 Ω 2% per PIPA B			
23	{ 4923370 L	Resistenza 220 Ω			
	{ 4933127 W	Resistenza 120 Ω 2% per PIPA B			
24	{ 4932925 K	Resistenza 82 Ω 2% per PIPA A			



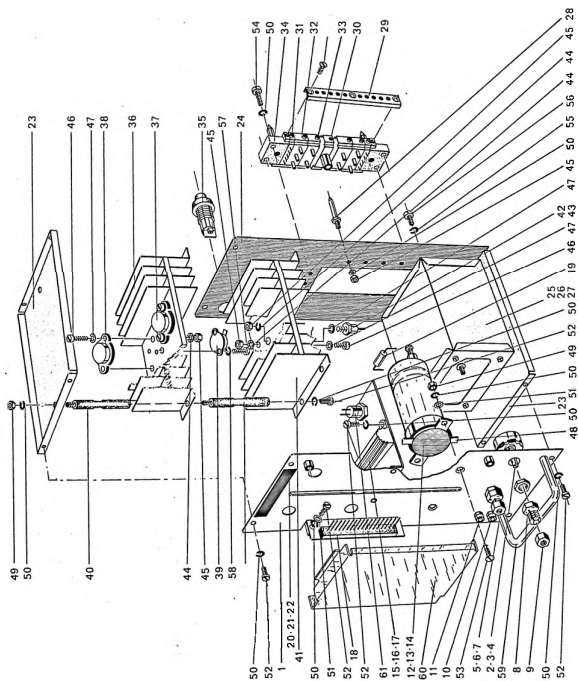
-	0620243 S	AG. Piastrina CIBO A	31	4924930 A	Resistenza 8,2 K Ω	- 0,25 W
-	0620242 V	AG. Piastrina CIBO B	32	4924290 R	Resistenza 1,8 K Ω	- 0,25 W
-	0620241 J	AG. Piastrina CIBO C	33	4934047 U	Resistenza 1 K Ω	- 0,5 W
1	531671 N	Transistor 2N1671A	34	4934405 T	Resistenza 2,4 K Ω	- 0,5 W
2	539081 W	Transistor BFY81	35	4933805 K	Resistenza 620 Ω	- 0,5 W
3	0000726 N	Transistor IW8916	36	4924450 R	Resistenza 2,7 K Ω	- 0,5 W
4	5333400 E	Transistor ZA398 B	37	4933725 S	Resistenza 510 Ω	- 0,5 W
5	5335750 N	Transistor 2N1711	38	4922930 R	Resistenza 82 Ω	- 0,25 W
6	0001434 A	Diodo P100	39	4933446 A	Resistenza 270 Ω	- 0,5 W
7	0000797 Z	Diodo 1X8998A	40	4923930 M	Resistenza 820 Ω	- 0,25 W
8	5826022 D	Diodo 1S2056		{ 4933607 J	Resistenza 390 Ω	- 0,5 W per CIBO A
9	5031710 Z	Condensatore 47 μ F 6 VL	41	{ 4934086 C	Resistenza 1,1 K Ω	- 0,5 W per CIBO B
10	5037730 C	Condensatore 47 μ F 20 VL		{ 4934287 T	Resistenza 1,8 K Ω	- 0,5 W per CIBO C
11	5041560 T	Condensatore 22 μ F 35 VL		{ 4933687 N	Resistenza 470 Ω	- 0,25 W per CIBO A
12	0000996 J	Condensatore 0,68 μ F 35 VL	42	{ 4934047 U	Resistenza 1 K Ω	- 0,25 W per CIBO B
13	5006308 R	Condensatore 1 K μ F 200 VL		{ 4934287 T	Resistenza 1,8 K Ω	- 0,25 W per CIBO C
14	5006776 T	Condensatore 10 K μ F 200 VL		{ 4932365 J	Resistenza 22 Ω	- 0,5 W per CIBO A
15	5011825 M	Condensatore 2,7 K μ F 200 VL	43	{ 4934367 K	Resistenza 2,2 K Ω	- 0,5 W per CIBO B
16	4962555 Y	Resistenza 33 Ω - 7 W		{ 0001004 L	Resistenza 5,6 K Ω	- 0,5 W per CIBO C
17	4962902 B	Resistenza 68 Ω - 3 W	44	{ 4934507 K	Resistenza 3,6 K Ω	- 0,5 W per CIBO B
18	4962198 V	Resistenza 22 Ω - 7 W		{ 4934847 L	Resistenza 6,8 K Ω	- 0,5 W per CIBO C
19	4923450 U	Resistenza 270 Ω - 0,25 W		{ 4922450 Y	Resistenza 27 Ω	- 0,25 W per CIBO A
20	4923050 V	Resistenza 100 Ω - 0,25 W	45	{ 4933245 J	Resistenza 160 Ω	- 0,5 W per CIBO B
21	4935285 P	Resistenza 18 K Ω - 0,5 W		{ 4933527 E	Resistenza 330 Ω	- 0,5 W per CIBO C
22	4924210 H	Resistenza 1,5 K Ω - 0,25 W	46	5041355 Q	Condensatore 6,8 μ F - 35 VL	
23	4923770 U	Resistenza 560 Ω - 0,25 W	47	5041160 K	Condensatore 2,2 μ F - 50 VL	
24	4924770 R	Resistenza 5,6 K Ω - 0,25 W		{ 5037500 R	Condensatore 15 μ F - 20 VL	
25	4922770 Y	Resistenza 56 Ω - 0,25 W	48	{ 4934207 X	Resistenza 1,5 K Ω - 2% per CIBO A	
26	4924532 W	Resistenza 3,3 K Ω - 0,25 W		{ 4934483 E	Resistenza 3 K Ω - 2% per CIBO B	
27	4934367 K	Resistenza 2,2 K Ω - 0,5 W	49	{ 0001004 L	Resistenza 5,6 K Ω - 2% per CIBO C	
28	4933887 B	Resistenza 750 Ω - 0,5 W		{ 5037270 W	Condensatore 4,7 μ F 20 V	
29	4935047 Y	Resistenza 10 K Ω - 0,5 W	50			
30	4922050 Z	Resistenza 10 Ω - 0,25 W				



box tensioni (ALI 150)

-	0842532 F	AG. Box +5	744 644
-	0842533 B	AG. Box +12	744 645
-	0842534 Y	AG. Box -20	744 646
1	0842893 G	Frontale	
2	4993540 C	Potenzionometro 10 K Ω 4W 10% (Box +12)	
3	4993540 C	Potenzionometro 10 K Ω 4W 10% (Box -20)	
4	4991070 W	Potenzionometro 5 K Ω 2W 10% (Box +5)	
5	4993305 A	Potenzionometro 330 Ω 2W 10% (Box +5)	
6	4993314 T	Potenzionometro 680 Ω 2W 10% (Box +12)	
7	4993340 Y	Potenzionometro 1,5 K Ω 2W 10% (Box -20)	
8	4999550 X	Boccola bloccaggio potenzionometro	
9	4999530 V	Dado bloccaggio potenzionometro	
10	5610021 W	Boccola pup rossa	
11	5610024 T	Boccola pup nera	
12	0001307 L	Condensatore 1000 μ F 40V (Box -20)	
13	5035679 S	Condensatore 6400 μ F 15V (Box +12)	
14	5035679 S	Condensatore 6400 μ F 15V (Box +5)	
15	4972904 R	Resistenza 60 Ω 50W 3% (Box -20)	
16	4971871 E	Resistenza 10 Ω 50W 3% (Box +12)	
17	4971086 B	Resistenza 2,5 Ω 50W 3% (Box +5)	
18	0620234 N	Piastrina con connettore	
19	5041355 Q	Condensatore 6,8 μ F 35V 20%	
20	0837923 X	Targhetta Box +5	
21	0837922 T	Targhetta Box +12	
22	0837921 P	Targhetta Box -20	
23	0837937 Z	Testata	
24	0837956 X	Pannello posteriore	
25	5421004 B	Induttanza 10 mH 5A (Box -20)	
26	5421002 J	Induttanza 5 mH 7A (Box +12)	
27	5421000 E	Induttanza 1 mH 15A (Box +5)	
28	0837931 Q	Spina	
29	0830512 X	Rotaia Souriau	

30	5616418 G	Estrattore femmina
31	5616450 D	Elemento maschio 5A
32	5616452 J	Elemento maschio 15A
33	5616454 B	Elemento maschio 25A
34	5616413 J	Squadra con guida
35	5141133 J	Pulsante RAFI
36	0837927 J	Dissipatore
37	5836002 R	Transistor 2N3713
38	5836000 C	Transistor 2N3772
39	5241302 W	Termostato Klixon
40	0838137 M	Bistabile
41	0837928 M	Dissipatore
42	5812010 W	Biodo IN1200 A (Box +12 -20)
43	5812012 B	Biodo controllato IN3999 (Box +5)
44	0683086 F	Rondella dentellata ϕ 4,2
45	0682260 E	Dado M4
46	0680550 G	Vite TC M4x15
47	0682456 X	Rondella piana ϕ 4,2
48	0001402 S	Fascetta condensatore
49	6321103 H	Dado M3
50	6321103 N	Rondella elastica ϕ 3,2
51	6331103 A	Rondella piana ϕ 3,2
52	6311230 Q	Vite TC M3x6
53	6312732 K	Vite TS M3x6
54	6311233 Z	Vite TC M3x12
55	6332104 B	Rondella elastica ϕ 4,2
56	6331243 S	Vite TC M4x10
57	0680116 G	Vite TC M2,6x8
58	0683040 M	Rondella elastica ϕ 2,8
59	0837519 E	Maniglia
60	0837160 R	Protezione
61	0001710 A	Biodo controllato 2N683



box ampliamento (ALI 150)

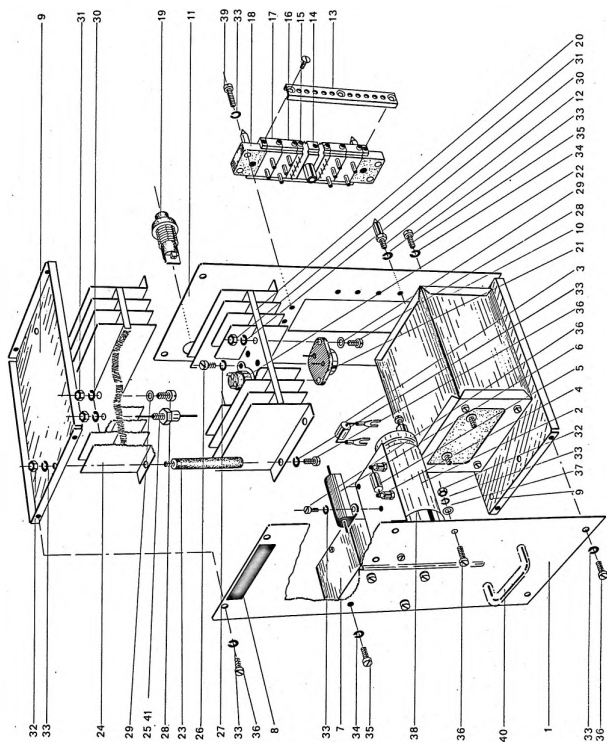
GE 115/3 · 120 · 130 - catalogo

AG. Box ampliamento 744 647

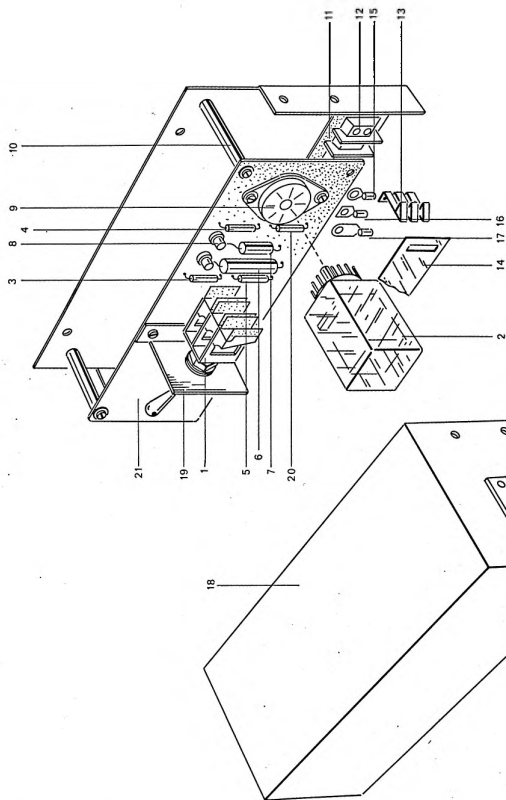
-	0842535 V
1	0842622 G
2	5035679 Z
3	5041355 Q
4	5613569 E
5	4962430 S
6	4971086 B
7	545226 Y
8	0837920 N
9	0837937 Z
10	5421000 E
11	0837952 W
12	0837931 Q
13	0830512 X
14	5616418 G
15	5616450 D
16	5616452 J
17	5616454 B
18	5616413 J
19	5141133 N
20	0837927 J
21	5836000 C
22	5241302 W
23	0838137 M
24	0837928 M
25	5812012 B
26	0680116 G
27	0683040 M
28	0680550 X
29	0682456 X
30	0683086 F
31	0682260 E

32	6321103 H
33	6332103 N
34	6332104 B
35	6311242 W
36	6311231 R
37	6331103 A
38	0001402 S
39	6311233 Z
40	0837519 X
41	5812010 W

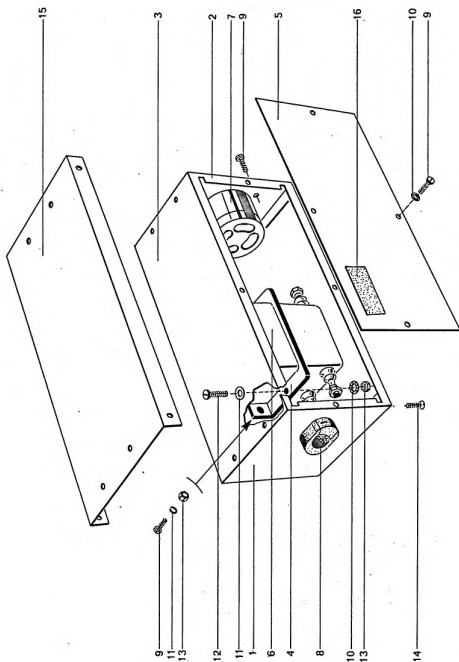
Dado M3
Rondella elastica ø 3,2
Rondella elastica ø 4,2
Vite TC M4x8
Vite TC M3x8
Rondella piana ø 3,2
Fascetta fissaggio cond.
Vite TC M3x12
Maniglia
Diodo SI 1M 1200 A per versione A normale



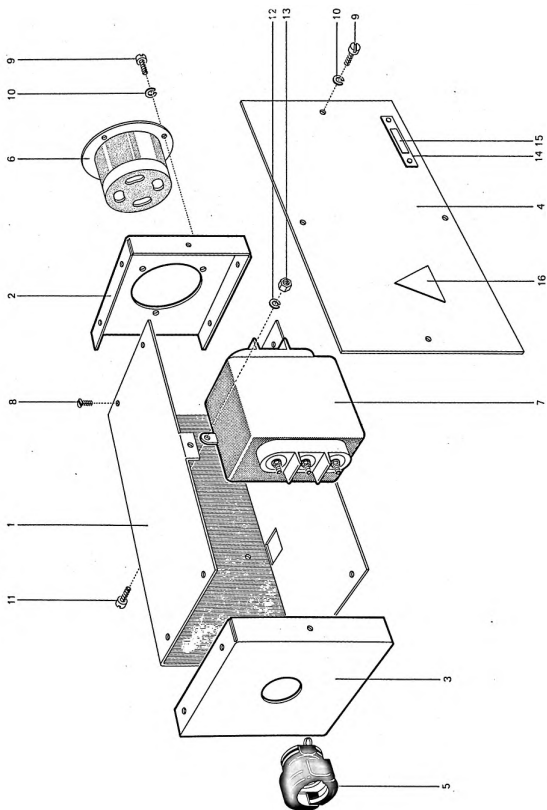
1	0001988 B	Interruttore
2	0001385 H	Relé Potter
3	4926050 S	Resistenza 100 K Ω
4	4922530 Y	Resistenza 33 Ω
5	4924130 H	Resistenza 1,2 K Ω
6	5037781 J	Condensatore 50 μ F
7	5037454 E	Condensatore 10 μ F
8	0000813 B	Transistore 1 W 8918
9	0001370 W	Zoccolo per relé
10	0838494 V	Distanziale
11	5612991 R	Piastrina numerata Rhodex
12	5612439 C	Morsetti Rhodex
13	0839653 U	Molletta tipo A
14	0839346 J	Piastrina isolante
15	5613350 W	Capocorda AMP
16	5613333 D	Capocorda AMP
17	5613329 W	Capocorda AMP
18	0842585 H	Copertura
19	0838491 Y	Squadretta Interruttore
20	4963551 T	Resistenza SECI 330 Ω
21	0832442 D	Supporto stampato



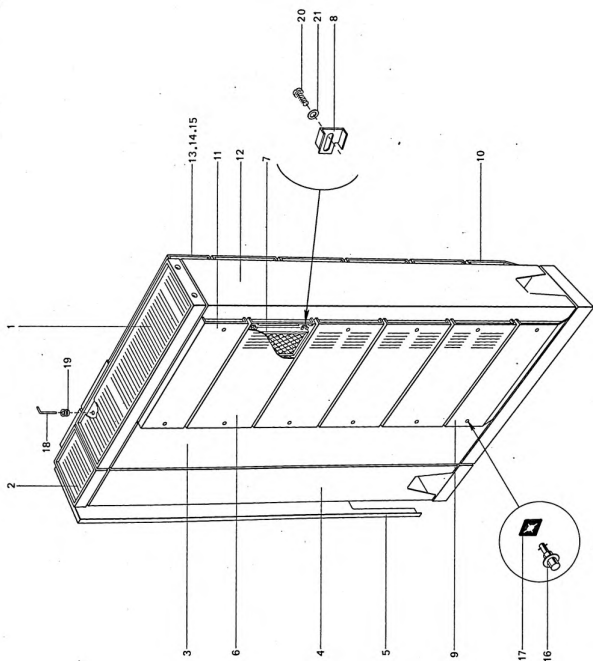
-	0645810	P	AG. ALI 290/A
1	0837774	U	Testata destra
2	0837773	F	Testata sinistra
3	0837775	Y	Fondo
4	0839167	L	Sostegno filtri
5	0842182	C	Coperchio con targhette
6	5427060	F	Filtro ICAR
7	0001292	K	Spina INLET
8	0001373	F	Passacavo
9	6311243	S	Vite TC 4Max10
10	6332304	F	Rondella dentellata ϕ 4,3
11	6331104	X	Rondella piana ϕ 4,3
12	6311245	K	Vite TC 4Max15
13	6321104	W	Dado 4MA
14	6312733	P	Vite TS 3Max8
15	0838499	S	Supporto ALI 290
16	0831766	S	Etichetta autoadesiva



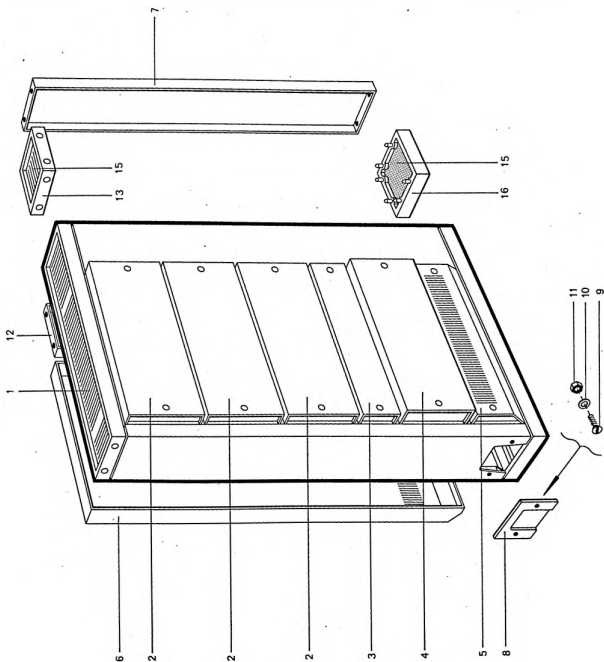
-	0643394	H	AG. ALI 290
1	0819152	L	Fondo
2	0837774	U	Testata DX
3	0837773	F	Testata SX
4	0839165	C	Coperchio
5	0001373	F	Passacavo
6	0001292	K	Connettore
7	5427068	F	Filtro
8	6312733	P	Vite TS 3x8
9	6311243	S	Vite TC 4x10
10	6332104	B	Rondella elastica ø 4,3
11	0680534	D	Vite TC 4x10 ottone
12	0683081	S	Rondella elastica ø 4,3 B8
13	0682260	E	Dado M4 ottone
14	0834397	W	Targhetta U.E.
15	0834416	U	Etichetta codice
16	3543106	X	Targhetta



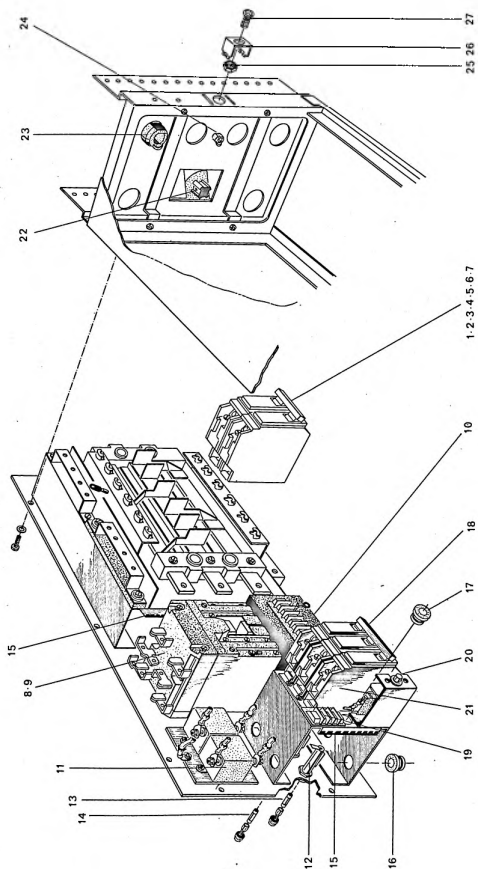
1	0835949 B	Coperchio grigliato superiore
2	0835830 D	Coperchio grigliato
3	0835852 L	Pannello piede
4	0835901 R	Pannello camino centrale
5	0835892 Z	Pannello camino centrale
-	0836507 M	AG. Copertura con feritoie
6	0836508 A	Coperchio
7	0001482 W	Filtro
8	0836871 N	Tassello fissaggio filtro
9	0835944 E	Coperchio piede
10	0835943 R	Coperchio piede
11	0836284 X	Coperchio $\frac{1}{2}$ modulo
12	0835975 B	Canaletto piede
-	0836293 B	AG. Coperchio $\frac{1}{2}$ modulo grigliato
13	0836290 S	Coperchio
14	0001481 J	Filtro
15	0836871 N	Tassello fissaggio filtro
16	0834661 Q	Pulsante CAMLOC
17	0834665 R	Staffa
18	0835863 R	Perno
19	9401020 E	Gommino
20	0836503 L	Vite 4Max10
21	6331104 X	Rondella piana ϕ 4,3



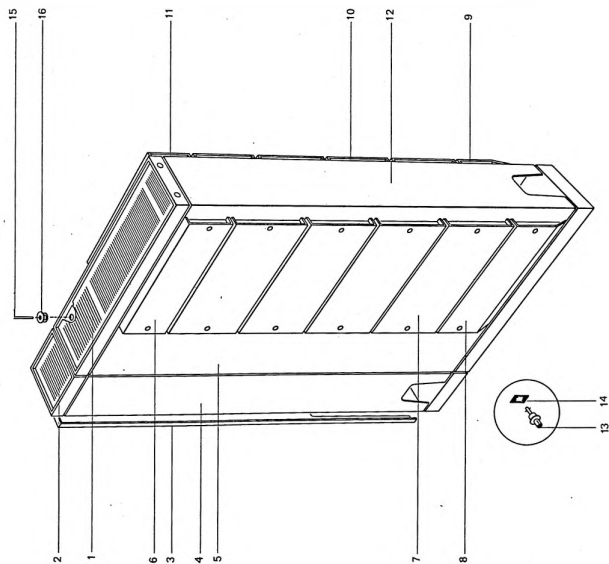
1	0817036 H	Coperchio superiore
2	0836262 U	Coperchio 1 mod.
3	0836286 F	Coperchio $\frac{1}{2}$ mod.
4	0674317 V	Coperchio 1 mod.
5	0835910 D	Coperchio 1 mod. piede
6	0674383 B	Coperchio lungo
7	0817075 Z	Pannello
8	0817043 D	Tappo
9	6312735 G	Vite T.S. 4x12
10	6331104 X	Rondella piana ϕ 4,3
11	6321104 W	Dado M4
12	0817045 W	Pannello per camino
13	0817073 G	Coperchio grigliato
14	0835835 F	Fondello piede
15	0817083 R	Giunzione anello sup.
16	0674268 M	Giunzione piede



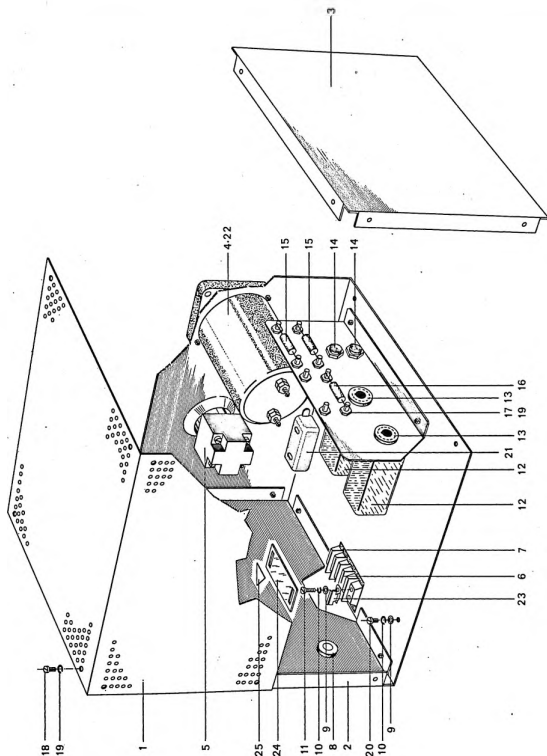
1	0001357 E	Breaker unipolare 10A
2	0001474 E	Breaker bipolare 10A
3	0001519 F	Breaker bipolare 15A
4	0002114 E	Breaker tripolare 10A
5	0001356 A	Breaker tripolare 15A
6	0002115 A	Breaker tripolare 20A
7	0001518 B	Breaker tripolare 30A
8	0001885 C	Contattore 24V - 50 Hz
9	0001884 G	Contattore 24V - 60 Hz
10	0001315 S	Trasformatore AROS
11	0001449 G	Filtro ICAR
12	0001238 X	Portafusibile Littelfuse
13	0001244 X	Fusibile 3A
14	0001218 V	Fusibile 0,5A
15	0001858 W	Passacavo Wechesser
16	0001875 T	Passacavo Bushing
17	0001876 F	Passacavo Bushing
18	0838666 W	Piastrina numerata
19	5612455 E	Morsettiera Rhodex
20	0001726 P	Pulsante Honeywell
21	0001355 W	Breaker TQC 3430 50 Hz
22	0001354 S	Spina INLET
23	0001373 F	Passacavo Bushing
24	0001875 T	Passacavo a scatto
-	0835484 X	A0. Supporto fissaggio coperchio
25	0834662 U	Dado Fastener
26	0835132 C	Supporto
27	0834663 Y	Ricettacolo



1	0835949 B	Coperchio grigliato superiore
2	0835830 D	Coperchio grigliato
3	0835972 Q	Pannello camino
4	0835901 R	Pannello camino
5	0835852 L	Pannello piede
6	0836278 P	Coperchio $\frac{1}{2}$ modulo
7	0836268 N	Coperchio 1 modulo
8	0835944 E	Coperchio piede
9	0835943 R	Coperchio piede
10	0836262 U	Coperchio 1 modulo
11	0836284 X	Coperchio $\frac{1}{2}$ modulo
12	0835875 B	Canaletta piede
13	0834661 Q	Pulsante CAMLOC
14	0834665 R	Staffa
15	0835863 R	Perno
16	9401020 E	Gommino



-	0646929 Z	AG. Contatore 60 Hz
-	0646705 M	AG. Contatore 50 Hz
1	0837614 U	Copertura di protezione
2	0837615 Y	Fiancata destra
3	0837616 C	Fiancata sinistra
4	0000898 H	Contatore G.E. 50 Hz
5	5168110 F	Interruttore a chiave
6	0001798 P	Morsettiera K 604/A
7	0001799 K	Piastrina numerata
8	0001366 B	Passacavo a semigusci
9	6331104 X	Rondella piana ϕ 4,3
10	6332104 B	Rondella elastica ϕ 4,3
11	6311245 K	Vite TC M4x15
-	0842673 H	AP. Assieme supporto relé
12	0001385 H	Relé Potter KAP 14 DY
13	0001370 W	Zoccolo AMPH
14	5027310 Z	Condensatore 0,1 μ F 1000 VDC
15	4963071 U	Resistenza RSN 100 Ω 3W
16	5822725 X	Diode EB 1361
17	5613569 E	Torretta Gregorini
18	6311231 R	Vite TC M3x8
19	6332103 A	Rondella elastica ϕ 3,2
20	6311243 S	Vite TC M4x10
21	5250102 Z	Protezione contatore
22	0001317 A	Contatore 60 Hz
23	0839653 U	Molletta Tp A
24	0839355 F	Piastrina isolante
25	3443104 P	Targhetta



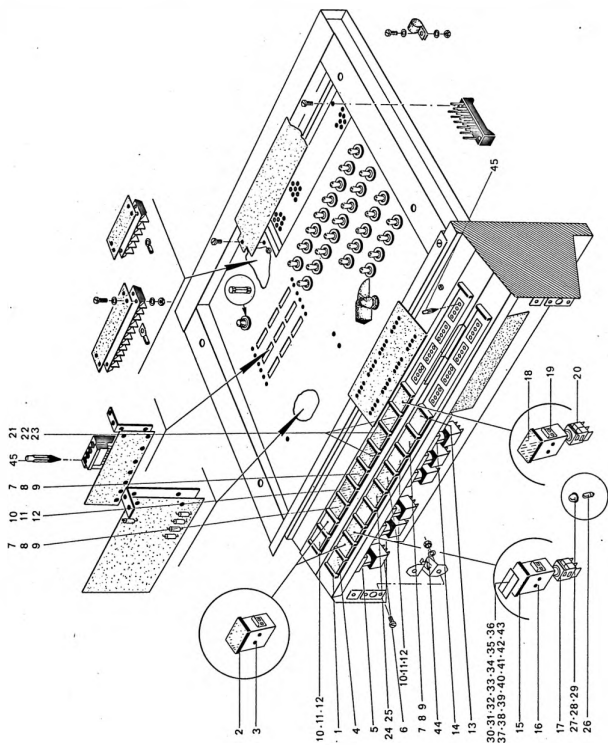
tele-console (TAV 421 B-C)

GE 115/3 · 120 · 130 - catalogo

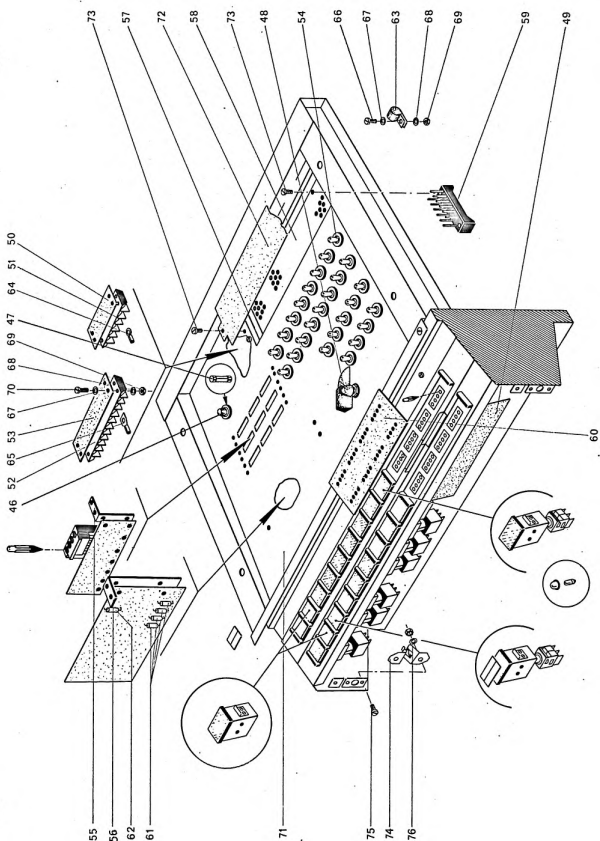
-	0646523 N	AG. Teleconsole Mod. B
1	0842512 D	Copertura scatola
2	0837979 N	Scatola
3	0838083 G	Distanziatore
4	0005135 Z	Calamita tipo 150 TBFM
5	0001150 Y	Separatore
6	0001367 F	Fermacavo a semiganci 19, 2x3, 3
7	0001823 D	Lampadino ASA 20 V
8	0839256 R	Targhetta STEP-BY-STEP
9	6321109 H	Dado M3
10	0842272 V	Tasto monostabile
11	0800796 H	Cavo
-	0842511 Z	AP. Piastrina resistenze
12	4924370 H	Resistenza 2,2 KΩ 1/4W
13	4923770 U	Resistenza 560Ω 1/4W
14	6311230 Q	Vite TC M3x6
15	6331103 A	Rondella piana ø 3,2
16	6332103 N	Rondella elastica ø 3,2
-	0842487 P	AP. Tasto stabile
17	0001155 S	Piastrina a un pezzo 2A70
18	0001148 W	Unità meccanica a 2 lampadine 2C1
19	0001152 D	Unità a comando stabile 2B26
20	0837980 U	Coperchio
-	0646021 X	AG. Teleconsole Mod. C
21	0842512 D	Copertura scatola
22	0837979 N	Scatola
23	0005135 Z	Calamita tipo 150 TBFM
24	0001150 Y	Separatore
25	0001366 F	Fermacavo a semiganci 20x3,2
26	0001823 D	Lampadino ASA 20V
27	0839256 R	Targhetta STEP-BY-STEP

28	6321109 H	Dado M3
29	0842272 V	Tasto monostabile
30	0800817 U	Cavo
31	6311231 R	Vite TC M3x8
32	6331103 A	Rondella piana ø 3,2
33	6332103 N	Rondella elastica ø 3,2
-	0842391 V	AP. Tasto bistabile
34	0001155 S	Piastrina a 3 pezzi
35	0001149 S	Unità indicatrice 4 lampad. 2C3
36	5141500 S	Unità ad azione alternata
37	0837980 U	Coperchio

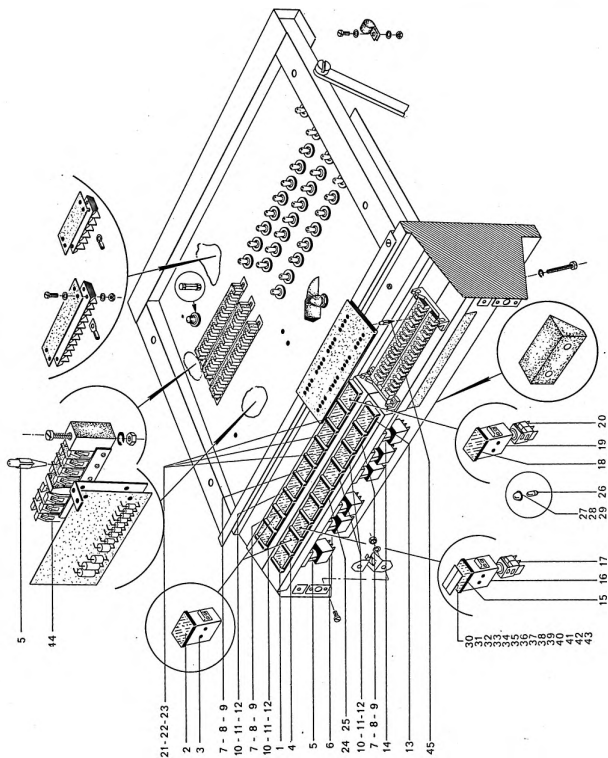
1	5141504 Y	Elemento separatore	19	0001149 S	Unità meccanica a 4 lampadine 2C3
-	0842262 V	AG. Assieme tasto finto	20	0001152 D	Unità a comando mantenuto 2D26
2	0001155 S	Piastrina un pezzo	-	0842487 P	AG. Interruttore stabile
3	0838879 H	Assieme saldatura supporto	21	0001155 S	Piastrina a un pezzo 2A70
-	0842261 Q	AG. Interruttore	22	0001148 W	Unità meccanica a 2 lampadine 2C1
4	0001157 A	Piastrina filtro rosso	23	0001152 D	Unità a comando mantenuto 2D26
5	0001149 S	Unità meccanica a 4 lampadine 2C3	-	0842218 R	AG. Indicatore luminoso
6	0001161 Z	Unità a comando momentaneo 2D2	24	0001156 E	Piastrina a 3 pezzi 2A65-2 sez. orizz.
-	0842214 Q	AG. Interruttore monostab. con separ.	25	0001154 W	Unità per indicatori luminosi 2F3
7	0001156 E	Piastrina a 3 pezzi 2A65-2 sez. orizz.	26	0001823 D	Lampadino CM8
8	0001149 S	Unità meccanica a 4 lampadine 2C3	27	0001160 Z	Cappuccio lampadine rosso
9	0001151 V	Unità a comando momentaneo 2D2	28	0001161 S	Cappuccio lampadine giallo
-	0842270 Q	AG. Interruttore monostabile	29	0001163 A	Cappuccio lampadine blu
10	0001155 S	Piastrina a 3 pezzi 2A70 sez. unica	30	0831823 L	Targhetta OPERATOR CALL
11	0001148 W	Unità meccanica a 2 lampadine 2C1	31	0839247 L	Targhetta LOAD - 1 / LOAD - 2
12	0001151 Z	Unità a comando momentaneo 2D2	32	0839254 H	Targhetta HALT - START
-	0842219 M	AG. Indicatore luminoso	33	0839256 R	Targhetta STEP BY STEP
13	0001155 S	Piastrina a 3 pezzi 2A70 sez. unica	34	0839257 M	Targhetta LOAD
14	0001154 W	Unità per indicatori luminosi 2F3	35	0839245 C	Targhetta SWITCH 2
-	0842216 Y	AG. Interruttore bistabile	36	0839255 D	Targhetta CLEAR
15	0001155 S	Piastrina a 3 pezzi 2A70 sez. unica	37	0839246 Q	Targhetta SWITCH 1
16	0001149 S	Unità meccanica a 4 lampadine 2C3	38	0839250 B	Targhetta POWER ON
17	0001152 D	Unità a comando mantenuto 2D26	39	0837665 V	Targhetta MEM CHECK - INV ADD
-	0842217 U	AG. Interruttore bistabile con separat.	40	0839244 G	Targhetta ALERT - POWER OFF
18	0001156 E	Piastrina a 3 pezzi 2A65-2 ass. orizz.	41	0831825 D	Targhetta MAINT - ON / LAMPS CHECK
			42	0831815 C	Targhetta ON
			43	0831792 C	Targhetta STAND BY
			44	6321103 H	Dado 3MA
			45	5361011 M	Lampadino 12V - 0,02A



46	0001238 X	Portafusibile LITTELFUSE	75	6311231 R	Vite TC 3Max8
47	0001253 B	Fusibile 10A - 250V	76	6331103 A	Rondella ø 3,2
48	5114404 Y	Commutatore JBT	<u>Elenco piastrine</u>		
49	0842253 X	Assieme lampadini	78	0616032 P	Piastrina FICO B
50	5612994 H	Piastrina numerata Rhodex 0505	79	0618033 C	Piastrina PONT ø M
51	5612430 A	Morsettiera Rhodex K 505/A	80	0615233 S	Piastrina TAPO D
52	5612438 H	Morsettiera Rhodex K 510/A			
53	5612987 L	Piastrina numerata Rhodex 0510			
54	0001942 D	Deviatore CUTLER			
55	0678338 M	Supporto			
56	0678339 R	Supporto			
57	0678337 Y	Supporto piastra connettori.			
58	0842264 M	Piastra connettori			
59	0834000 S	Connettore maschio			
60	0678553 D	Maschera lampadini			
-	0620284 R	AG. Supporto resistenza			
61	0001510 C	Resistenze 27 $\frac{1}{4}$ W			
62	5003635 L	Condensatore 0,47 µF			
63	5618054 V	Serracavo Looping tipo 2			
64	5613350 W	Capocorda AMP			
65	5613333 D	Capocorda AMP			
66	6311244 P	Vite TC 4Max2			
67	6331104 X	Rondella piana ø 4,3			
68	6332104 D	Rondella elastica ø 4,3			
69	6321104 W	Dado 4MA			
70	6311247 T	Vite TC 4Max20			
71	0678556 A	Piastra console manutenzione			
72	0678471 V	Piastra copri pins			
73	6307430 Q	Vite TC 3Max6			
74	0005316 F	Molletta			

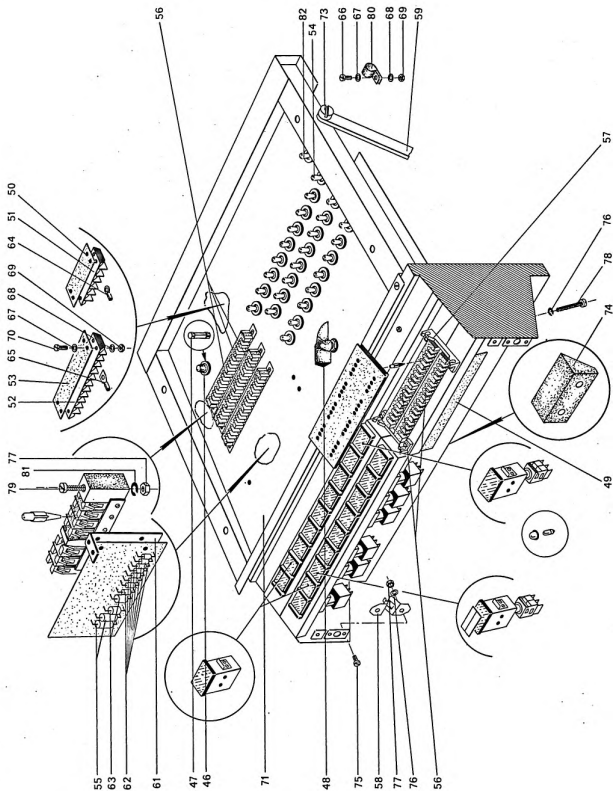


1	5141504 Y	Elemento separatore	19	0001149 S	Unità meccanica a 4 lampadine 2C3
-	0842262 V	AG. Assegno tasto finto	20	0001152 D	Unità a comando mantenuto 2D26
2	0001155 S	Piastrina un pezzo	-	0842487 P	AG. Interruttore stabile
3	0838879 H	Assieme saldatura supporto	21	0001155 S	Piastrina a un pezzo 2A70
-	0842261 Q	AG. Interruttore	22	0001148 W	Unità meccanica a 2 lampadine 2C1
4	0001157 A	Piastrina filtro rosso	23	0001152 D	Unità a comando mantenuto 2D26
5	0001149 S	Unità meccanica a 4 lampadine 2C3	-	0842218 R	AG. Indicatore luminoso
6	0001161 Z	Unità a comando momentaneo 2D2	24	0001156 E	Piastrina a 3 pezzi 2A65-2 sez. orizz.
-	0842214 Q	AG. Interruttore monostabile con separ.	25	0001154 W	Unità per indicatori luminosi 2F3
7	0001156 E	Piastrina a 3 pezzi 2A65-2 sez. orizz.	26	0001823 D	Lampadino CM8
8	0001149 S	Unità meccanica a 4 lampadine 2C3	27	0001160 Z	Cappuccio lampadine rosso
9	0001151 V	Unità a comando momentaneo 2D2	28	0001161 S	Cappuccio lampadine giallo
-	0842270 Q	AG. Interruttore monostabile	29	0001163 A	Cappuccio lampadine blu
10	0001155 S	Piastrina a 3 pezzi 2A70 sez. unica	30	0831823 L	Targhetta OPERATOR CALL
11	0001148 W	Unità meccanica a 2 lampadine 2C1	31	0839247 L	Targhetta LOAD - 1 / LOAD - 2
12	0001151 Z	Unità a comando momentaneo 2D2	32	0839254 H	Targhetta HALT - START
-	0842219 M	AG. Indicatore luminoso	33	0839256 R	Targhetta STEP BY STEP
13	0001155 S	Piastrina a 3 pezzi 2A70 sez. unica	34	0839257 M	Targhetta LOAD
14	0001154 W	Unità per indicatori luminosi 2F3	35	0839245 C	Targhetta SWITCH 2
-	0842216 Y	AG. Interruttore bistabile	36	0839255 D	Targhetta CLEAR
15	0001155 S	Piastrina a 3 pezzi 2A70 sez. unica	37	0839246 Q	Targhetta SWITCH 1
16	0001149 S	Unità meccanica a 4 lampadine 2C3	38	0839250 B	Targhetta POWER ON
17	0001152 D	Unità a comando mantenuto 2D26	39	0837665 V	Targhetta MEM CHECK - INV ADD
-	0842217 U	AG. Interruttore bistabile con separ.	40	0839244 G	Targhetta ALERT - POWER OFF
18	0001156 E	Piastrina a 3 pezzi 2A65-2 sez. orizz.	41	0831825 D	Targhetta MAINT - ON / LAMPS CHECK
			42	0831815 C	Targhetta ON
			43	0831792 C	Targhetta STAND BY
			44	0837278 K	Supporto lampadine
			45	5361011 M	Lampadino 12V - 0,02A

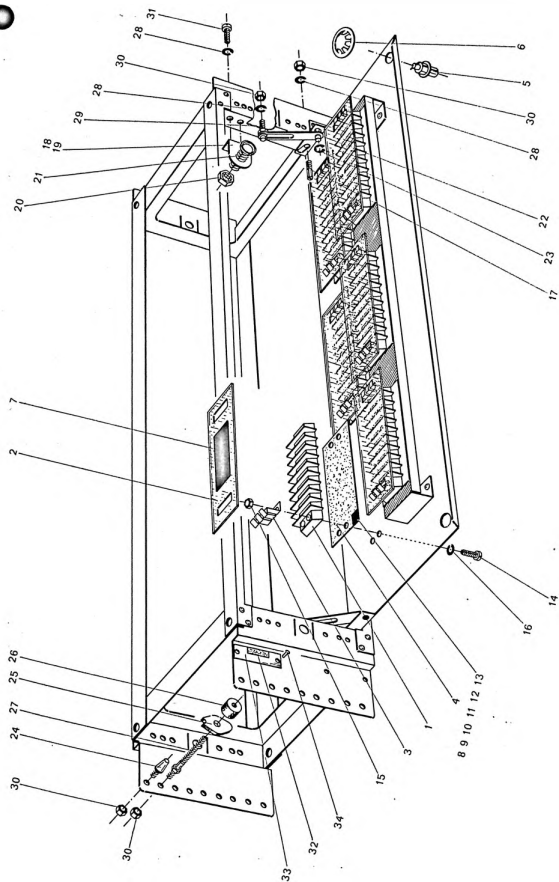


46	0001238 X	Portafusibile LITTELFUSE			
47	0001523 B	Fusibile 10A - 250 V			
48	5114404 Y	Commutatore JBT			
49	0837278 K	Assieme lampadini			
50	5612994 H	Piastrina numerata Rhodex Ø505			
51	5612430 B	Morsettiera Rhodex K 505/A			
52	5612438 H	Morsettiera Rhodex K 510/A			
53	5612987 L	Piastrina numerata Rhodex Ø510			
54	0001942 D	Deviatore CUTLER			
55	0678338 M	Supporto resistenze			
56	0837398 X	Copri lampadini			
57	0679923 X	Innesto per masohera lampadini			
58	0005316 F	Molletta			
59	0678450 S	Braccio d'arresto			
60	0679922 T	Maschera lampadini			
-					
61	0001510 C	AG. Piastrina LAFI			
62	5003635 L	Resistenze 27 $\frac{1}{4}$ W			
63	5037781 S	Condensatore 0,47 μ F			
		Condensatore 50 μ F - 25 VL			
64	5613350 W	Capocorda AMP			
65	5613333 D	Capocorda AMP			
66	6311244 P	Vite TC 4Max12			
67	6331104 X	Rondella piana Ø 4,3			
68	6332104 B	Rondella elastica Ø 4,3			
69	6321104 W	Dado 4MA			
70	6311247 T	Vite TC 4Max20			
71	0678556 A	Piastra console manutenzione			
72	0678471 V	Piastra copri pins			
73	0678470 U	Studs			
74	0679924 L	Tassello di battuta			

75	6311231 R	Vite TC 3Max8
76	6331103 A	Rondella Ø 3,2
77	6321103 H	Dado 3MA
78	7454744 G	Vite TC M3x35
79	7454746 Q	Vite TC M3x40
80	5618054 W	Serracavo looping tipo 2
81	6332103 N	Rondella elastica Ø 3,2
82	5111222 L	Deviatore VEAM bipolare



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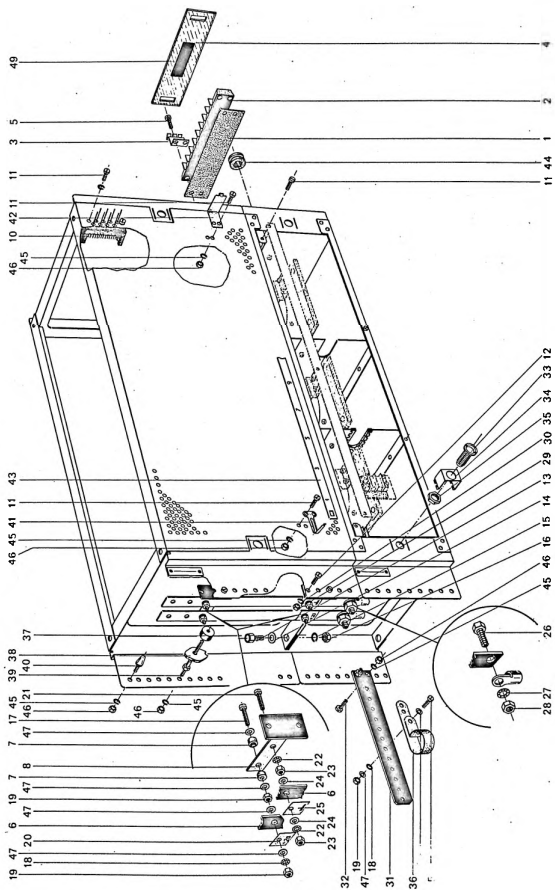


1	5612989 R	Piastrina numerata Rhodex
2	5612544 B	Morsetti Rhodex
3	0839653 U	Molletta tipo A
4	0839360 E	Protezione morsetti
5	6311247 T	Vite TC M4x20
6	0839716 X	Barra di alimentazione
7	0834229 E	Boccola isolante
8	0839939 B	Supporto barre alimentazione
9	0836264 M	Coperchio per stizopor
10	0834000 S	Connettore maschio
11	6307430 Q	Vite TC 3Max6
12	0680220 V	Vite TC M3x10
13	6313132 B	Vite TCE M5x15
14	6331105 T	Rondella piana ø 5,3
15	6332105 F	Rondella elastica ø 5,3
16	6321105 S	Dado M5
17	6311248 Q	Vite TC M4x25
18	6332104 X	Rondella elastica ø 4,3
19	6321104 W	Dado M4
20	0831095 U	Targhetta +20
21	0680551 F	Vite TC M4x18
22	0683086 F	Rondella elastica ø 4,3
23	0682260 E	Dado esagonale M4
24	0682456 X	Rondella piana ø 4,3
25	0831096 G	Targhetta 0
26	6314145 N	Vite TE M8x20
27	0683131 E	Rondella ø 8,4
28	0682481 V	Dado M8
29	0682160 C	Dado M3
30	0683066 W	Rondella dentellata ø 3,2
31	0834189 J	Bandella reggicavi
32	6311232 V	Vite TC M3x10

33	0834663 Y	Ricettacolo
34	0835132 C	Supporto
35	0834662 X	Dado Fastener
36	5618056 D	Serracavo Looping tipo 3
37	0839610 P	Blocca cavo zigrinato
38	0839612 U	Premicavo
39	0839609 V	Tirante
40	0839611 Q	Colonnina
41	0839474 P	Supporto a balestra sinistro
42	0839473 S	Supporto a balestra destro
43	0839772 W	Riga numerata per pacchi
44	0001876 F	Passacavo
45	6331103 N	Rondella elastica ø 3,2
46	6321103 H	Dado M3
47	6331104 X	Rondella piana ø 4,3
48	0836293 B	Coperchio ventilatore
49	0831766 S	Targhetta

NOTA : Per il VAR 321 Vedi a pag. 6

NOTE : For VAR 321 see page 6



SIN 460

1	0611313 Z	Piastrina ROCA
2	0615211 Q	Piastrina CAP 2
3	0615217 Z	Piastrina CAP 4
4	0618011 S	Piastrina FACI
5	0616033 K	Piastrina FICO A
6	0612021 H	Piastrina FLIP B
7	0611429 W	Piastrina INCA E
8	0611428 S	Piastrina INPO E
9	0611520 V	Piastrina INZE
10	0611511 V	Piastrina NORR CA
11	0611510 U	Piastrina NORR DS
12	0618012 E	Piastrina PONT A

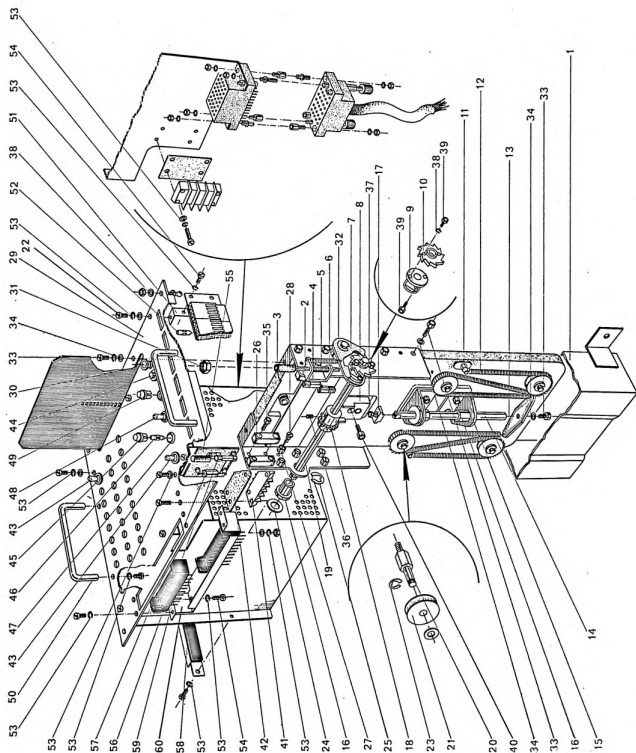
MEM 480

1	0610082 N	Piastrina LIRI 2C
2	0610084 F	Piastrina LIRI 2E
3	0610027 D	Piastrina OEMA 24
4	0610083 J	Piastrina LIRI 2D
5	0610081 A	Piastrina LIRI 2B
6	0610054 U	Piastrina PIME 2A
7	0610059 Z	Piastrina REDI 2A
8	0610070 Y	Piastrina TEME 2A
9	0610051 X	Piastrina NAME 2A
10	0610002 J	Piastrina AMPL 2A
11	0610030 U	Piastrina INTE 2A
12	0610029 W	Piastrina-INIB 2A
13	0610063 C	Piastrina REIN 2A
14	0610037 E	Piastrina LOGI 2B
15	0610036 A	Piastrina LOGI 2A
16	0610031 V	Piastrina INTE 2B
17	0610053 F	Piastrina PATE 2A
18	0610025 V	Piastrina FILT 2B
19	0610026 H	Piastrina FILT 2C
20	0610213 W	Piastrina FORL 2A
21	0610208 X	Piastrina VIMA 2A
22	0610211 N	Piastrina VILE 2A

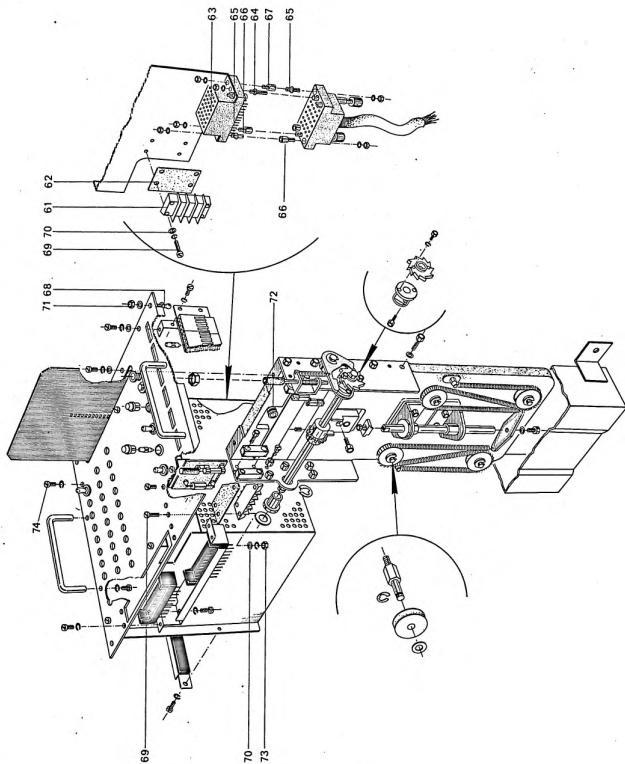
prova piastre (VAR 380)

-	0646702 Y	AG. Prova piastre
-	0842713 D	AP. Lettore schede
1	0837046 C	Scatola protezione
-	0842777 C	AP. Contatti
2	5300060 W	Contatto
3	0837033 E	Pulsante
4	0837032 A	Supporto pulsante
5	0837036 B	Molla pulsante
6	0837039 Y	Molla scappamento
7	0837020 Y	Bilanciere
8	0837028 T	Pattino
9	0837171 K	Mozzo
10	0837023 D	Ingranaggio per avanzamento
11	0837030 Y	Portamolli
12	0837019 W	Molla caricamento schede
13	0837016 H	Piastrina attacco molle
14	0837015 X	Asta guida schede
15	0819158 E	Supporto con bronzina
16	0000977 C	Bronzina
17	0837014 Z	Piastrina appoggio scheda
18	0837026 A	Ingranaggio ferma scheda
19	0837025 W	Albero comando
20	0837029 X	Ferno puleggia
21	0809568 H	Puleggia
22	6311231 R	Vite TC M3x8
23	6337109 D	Anello benzina
24	6331108 Y	Rondella
25	6337114 V	Anello benzina ø 8
26	0837011 U	Guida rettilinea
27	0837012 G	R-llino guida schede
28	0837013 C	Stud porta rullino
29	0837534 U	Frontale

30	0837037 F	
31	0837038 U	
32	6337111 X	Anello Benzina ø 6
33	6313115 W	Vite TCE
34	6331104 X	Rondella ø 4,3
35	6313100 F	Vite TCE M3x6
36	6316110 Z	Vite STCE M4
37	6313710 G	Vite TSCE M4
38	6332104 B	Rondella elastica ø 4,3
39	7454756 R	Vite 3,5Mx10
40	6313104 D	Vite TCE M3x15
41	0000849 Y	Morsettiera Rhodex K 504/A
42	0000850 W	Piastrina numerata
43	0001942 D	Deviatore 2 vie - 2 posizioni
44	5141201 N	Pulsante unipolare Crouz rosso
45	5363152 W	Gemma rossa
46	5361011 M	Lampadino 12 V - 20 mA
47	5363150 R	Portalampe RAFI
48	5104040 W	Deviatore 2 posizioni - 3 vie
49	5363153 S	Gemma gialla
50	0837540 X	Maniglia
-	0842706 M	AP. Supporto lampadini
51	0837544 V	Squadretta
52	5361011 M	Lampadino 12 V - 20 mA
53	6332103 M	Rondella elastica ø 3,2
54	6311230 Q	Vite TC M3x6
-	0842740 X	AP. Piastrina di protezione
55	0837478 X	Protezione fusibile
56	0001259 V	Fusibile 1A 250 V
57	4961072 Y	Resistenza 1Ω 3W
58	0837541 Y	Traversino bloccaggio piastrine
59	0834000 S	Connettore maschio
60	0836890 W	Supporto connettori



61	5612404 R	Morsettiara Rhodex K 503/1
62	0001448 C	Piastrina numerata
63	0000730 H	Blocchetto 34 contatti AMP
64	0001123 E	Maschio accoppiamento centrale
65	0001102 L	Guida d'angolo maschio
66	0001124 T	Femmina di accoppiamento centrale
67	0001103 Q	Guida d'angolo femmina
68	0678508 A	Perno
69	6311234 N	Vite TC M3x15
70	6331103 N	Rondella piana ϕ 3,2
71	6322104 A	Dado cieco M4
72	0877041 T	Passacavo
73	6221103 H	Dado M3



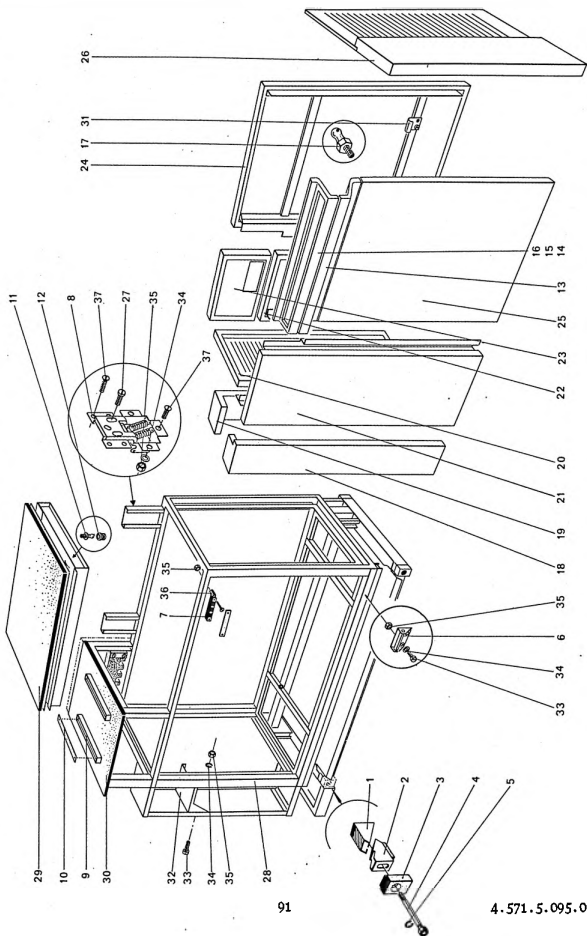
VAR 380

1	0837476 E	Scheda prova ANDO 2A	33	0837444 T	Scheda prova LOSE 2A
2	0816165 A	Scheda prova CAIN 2A	34	0837443 E	Scheda prova LOSE 2B
3	0837474 W	Scheda prova CAIN 2B	35	0837442 A	Scheda prova LOSE 2C
4	0837473 M	Scheda prova CANA 2A	36	0837441 W	Scheda prova LOSE 2D
5	0837472 D	Scheda prova CANA 2B	37	0837440 V	Scheda prova LOSE 2E
6	0837471 Z	Scheda prova CANA 2C	38	0837439 X	Scheda prova LOSE 2G
7	0837470 Y	Scheda prova CISP 2A	39	0837438 T	Scheda prova LOSE 2H
8	0837469 S	Scheda prova COFA 2A	40	0837437 E	Scheda prova LOSE 2L
9	0837468 W	Scheda prova CONT 2A I	41	0837436 A	Scheda prova LOSE 2M
10	0837467 H	Scheda prova CONT 2A II	42	0837435 W	Scheda prova NONA 2A
11	0837466 D	Scheda prova COVE 2A	43	0837434 S	Scheda prova NONE 2A
12	0837465 Z	Scheda prova DECO 2A I	44	0837433 D	Scheda prova NONI 2A
13	0837464 V	Scheda prova DECO 2A II	45	0837432 H	Scheda prova ORCA 2A
14	0837463 G	Scheda prova DEEC 2A	46	0837431 V	Scheda prova RECE 2A
15	0837462 C	Scheda prova DEFO 2A	47	0837430 U	Scheda prova RECO 2A
16	0837461 Y	Scheda prova DEFO 2B	48	0837429 W	Scheda prova RECS 2A
17	0837460 X	Scheda prova DERO 2A I	49	0837428 S	Scheda prova RECU 2A
18	0837459 Z	Scheda prova DERO 2A II	50	0837427 D	Scheda prova RENO 2A
19	0837458 V	Scheda prova DESA 2A	51	0837426 H	Scheda prova REPA 2A
20	0837457 G	Scheda prova DESA 2B	52	0837425 V	Scheda prova RESI 2A
21	0837456 C	Scheda prova DESA 2C	53	0837424 Z	Scheda prova RIIN 2A
22	0837455 Y	Scheda prova DEVA 2A	54	0837423 C	Scheda prova SEBO 2A
23	0837454 U	Scheda prova ESCO 2A	55	0837422 G	Scheda prova STOL 2A
24	0837453 F	Scheda prova FIFA 2A	56	0837421 U	Scheda prova TISE 2A
25	0837452 B	Scheda prova FILC 2A	57	0837420 J	Scheda prova TISE 2B I
26	0837451 X	Scheda prova INFE 2A	58	0837419 V	Scheda prova TISE 2B II
27	0837450 W	Scheda prova INVE 2A	59	0837418 Z	Scheda prova TRIN 2A
28	0837449 Y	Scheda prova LOBO 2A	60	0837417 C	Scheda prova UARO 2A
29	0837448 U	Scheda prova LOBO 2B	61	0837416 G	Scheda prova UARI 2A I
30	0837447 F	Scheda prova LOGI 2A	62	0837415 U	Scheda prova UARI 2A
31	0837446 B	Scheda prova LOGI 2B	63	0837414 Y	Scheda prova VARI 2A
32	0837445 X	Scheda prova LOGI 2C	64	0837413 B	Scheda prova VARI 2B
			65	0837412 F	Scheda prova VIAL 2A

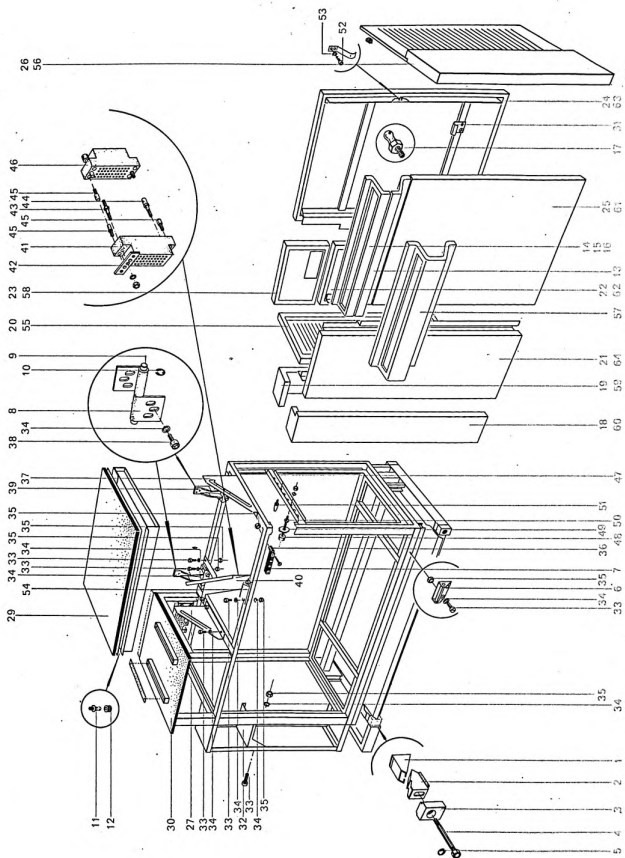
Elenco piastrine VAR 380

- 1 0610078 X Piastrina COMA 2A
- 2 0610025 V Piastrina FILT 2B
- 3 0610077 A Piastrina FULO 2A

1	0834614 Q	Cuneo superiore	33	6313114 S	Vite TCE M4x8
2	0834616 Y	Cuneo in gomma	34	7465706 V	Rondella piana ø 4,3
3	0834618 R	Tassello d'estremità	35	0682871 D	Dado 4MA
4	0834619 M	Vite di regolazione	36	0678509 E	Distanziale per magneti
5	6337116 D	Anello elastico ø 8	37	6312743 Q	Vite TS M4x8
6	0678370 J	Appoggio gancio			
7	6478500 M	Magnete			
8	0005324 Y	Cerniera a molla			
9	0678345 R	Appoggio Modem			
10	0678341 Q	Piastrina appoggio Modem			
11	0678508 A	Scrocco			
12	9431035 Y	Gommino			
13	0678416 C	Guscio inferiore			
14	0678417 G	Guscio superiore con scritta OGE			
15	0678434 W	Guscio superiore con scritta BOE			
16	0678436 E	Guscio superiore senza scritta			
17	0005317 B	Scrocco SRV			
18	0678566 B	Elemento di collegamento anteriore			
19	0678567 F	Elemento di collegamento posteriore			
20	0678345 Q	Pannello laterale grigliato sinistro			
21	0678552 H	Porta anteriore sinistra			
22	0678550 U	Porta posteriore sinistra			
23	0678563 F	Pannello fisso			
24	0678551 V	Porta posteriore destra			
25	0678549 W	Porta anteriore destra			
26	0674335 P	Pannello laterale destro			
27	6311243 S	Vite TC M4x10			
28	0678514 W	Struttura			
29	0678422 C	Formicone elemento asportabile			
30	0678421 Y	Formicone elemento asportabile			
31	0678371 K	Gancio			
32	0679908 X	Sostegno trasformatore			



1	0834614 Q	Cuneo superiore	34	7465706 V	Rondella piana ϕ 4,3
2	0834616 Y	Cuneo in gomma	35	0682871 D	Dado M4
3	0834618 R	Tassello d'estremità	36	0678509 E	Distanziale per magneti
4	0834619 M	Vite di regolazione	37	0678598 F	Supporto braccio d'arresto
5	6337116 D	Anello elastico ϕ 8	38	6313115 W	Vite TCE M4x10
6	0678370 J	Appoggio gancio	39	0679902 D	Montante per cerniera
7	6478500 M	Magnete	40	0679903 H	Piastrella supporto connettori
8	0678599 B	Cerniera	41	0001703 U	Bloccetto 50 contatti
9	0679900 Y	Perno per cerniera	42	0000730 N	Bloccetto 34 contatti
10	6337107 L	Anello elastico ϕ 5	43	0838039 M	Barretta fissaggio connettori
11	0678508 A	Scrocco	44	0001102 L	Guida d'angolo maschio
12	9431035 Y	Gommino	45	0001124 E	Femmina di accoppiamento
13	0678416 C	Guscio inferiore	46	0001103 Q	Guida d'angolo femmina
14	0678417 G	Guscio superiore con scritta OOE	47	0643044 F	Tappo tipo A 34 contatti
15	0678434 W	Guscio superiore con scritta BOE	48	0643045 B	Tappo tipo B 34 contatti
16	0678436 E	Guscio superiore senza scritta	49	0679907 A	Traversa reggicavi
17	0005317 B	Scrocco SRV	50	0839610 P	Blocca cavo zigrinato
18	0679911 N	Elemento di collegamento anteriore	51	0839612 U	Premicavo
19	0679910 M	Elemento di collegamento posteriore	52	0839609 V	Tirante
20	0674345 Q	Pannello laterale grigliato sinistro	53	0839611 Q	Colonnina
21	0817814 P	Porta anteriore sinistra	54	0860205 H	Vite 3x8 ottone
22	0817812 W	Porta posteriore sinistra	55	0683060 P	Rondella piana ϕ 3,2 ottone
23	0678413 F	Pannello fisso	56	0679906 E	Battuta console
24	0817813 S	Porta posteriore destra	57	0817004 A	Pannello laterale SX
25	0817815 K	Porta anteriore destra	58	0817011 S	Pannello laterale DX
26	0674335 P	Pannello laterale destro	59	0679957 T	Guscio lungo
27	0678586 M	Supporto braccio d'arresto	60	0817007 N	Pannello fisso
28	0678581 G	Struttura	61	0817810 R	Pannello posteriore di coll.
29	0678422 C	Formicone elemento asportabile	62	0817811 J	Pannello anteriore di coll.
30	0678561 W	Formicone elemento asportabile	63	0676330 X	Pannello anteriore DX
31	0678371 K	Gancio	64	0676329 X	Pannello posteriore SX
32	0679908 X	Sostegno trasformatore		0676322 H	Pannello posteriore DX
33	6313114 S	Vite TCE M4x8		0676328 T	Pannello anteriore SX



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Codice	Pag.	Rif.
0000647J	78	34
0000702X	28	10
0000711C	28	9
0000711N	34	3
0000726N	28	18
0000726R	32	95
0000726N	34	39
0000726N	46	3
0000730H	86	63
0000730N	92	41
0000765E	30	51
0000797Z	46	7
0000813B	28	16
0000813B	52	8
0000849Y	84	41
0000850W	84	42
0000882N	30	54
0000883J	18	34
0000883J	20	20
0000883J	30	28
0000898H	18	1
0000898H	66	4
0000977C	84	16
0000996J	46	12
0001004L	46	43
0001004L	46	49
0001102L	86	65
0001102L	92	43
0001103Q	86	67
0001103Q	92	45
0001123E	8	14
0001123E	86	64
0001124T	8	15
0001124T	86	66
0001124E	92	44
0001129Y	20	22
0001129Y	36	12
0001148W	68	18
0001148W	70	11
0001148W	70	22
0001148W	74	11
0001148W	74	22
0001149S	68	35
0001149S	70	5
0001149S	70	8
0001149S	70	16
0001149S	70	19
0001149S	74	5

Codice	Pag.	Rif.
0001149S	74	8
0001149S	74	16
0001149S	74	19
0001150Y	68	5
0001150Y	68	24
0001151V	70	9
0001151Z	70	12
0001151V	74	9
0001151Z	74	12
0001152D	68	19
0001152D	70	17
0001152D	70	20
0001152D	70	23
0001152D	74	17
0001152D	74	20
0001152D	74	23
0001154W	70	14
0001154W	70	25
0001154W	74	14
0001154W	74	25
0001155S	68	17
0001155S	68	34
0001155S	70	2
0001155S	70	10
0001155S	70	13
0001155S	70	15
0001155S	70	21
0001155S	74	2
0001155S	74	10
0001155S	74	13
0001155S	74	15
0001155S	74	21
0001156E	70	7
0001156E	70	18
0001156E	70	24
0001156E	74	7
0001156E	74	18
0001156E	74	24
0001157A	70	4
0001157A	74	4
0001160Z	70	27
0001160Z	74	27
0001161Z	70	6
0001161S	70	28
0001161Z	74	6
0001161S	74	28
0001163A	70	29
0001163A	74	29

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Codice	Pag.	Rif.
0001218V	62	14
0001238X	18	24
0001238X	24	17
0001238X	36	14
0001238X	38	4
0001238X	62	12
0001238X	72	46
0001238X	76	46
0001244X	62	13
0001250S	38	3
0001252F	36	15
0001253B	72	47
0001255U	36	16
0001257C	42	18
0001257C	44	1
0001258Z	36	17
0001258Z	42	19
0001258Z	44	26
0001259V	24	18
0001259V	28	15
0001259F	34	2
0001259V	84	56
0001261U	8	41
0001261V	18	25
0001261U	28	44
0001290E	18	35
0001292E	30	29
0001292K	36	22
0001292K	54	7
0001292K	56	6
0001296L	20	19
0001299H	32	71
0001307L	18	17
0001307M	32	62
0001307L	48	12
0001309D	18	18
0001309D	24	15
0001312D	36	8
0001315S	62	10
0001316E	30	12
0001316E	36	4
0001317A	18	2
0001317A	66	22
0001320Z	32	63
0001324X	38	7
0001354S	62	22
0001355W	62	21
0001356A	62	5

Codice	Pag.	Rif.
0001357E	62	1
0001366B	66	8
0001366F	68	25
0001367F	68	6
0001370W	20	18
0001370W	32	74
0001370W	40	79
0001370W	52	9
0001370W	66	13
0001373F	54	8
0001373F	56	5
0001373F	62	23
0001385H	52	2
0001385H	66	12
0001386M	32	76
0001386M	38	1
0001394R	30	4
0001394E	38	2
0001402S	18	19
0001402S	32	64
0001402S	38	24
0001402S	48	48
0001402S	50	38
0001426R	8	12
0001434A	22	31
0001434A	32	73
0001434B	34	33
0001434A	42	1
0001434A	42	23
0001434A	44	4
0001434A	46	6
0001448C	86	62
0001449G	62	11
0001474E	62	2
0001481B	10	33
0001481J	12	6
0001481J	14	9
0001481J	58	14
0001482W	14	33
0001482W	58	7
0001497U	10	21
0001499M	10	20
0001501Q	42	7
0001501Q	44	2
0001506V	24	10
0001510C	72	61
0001510C	76	61
0001518B	62	7

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Codice	Pag.	Rif.
0001519F	62	3
0001523B	76	47
0001605V	20	11
0001614C	10	1
0001614C	38	47
0001621G	20	8
0001663L	32	75
0001663L	38	15
0001674A	18	15
0001676J	18	14
0001680H	20	23
0001680N	32	66
0001682S	36	9
0001699R	8	13
0001700K	8	16
0001703U	92	41
0001710A	48	61
0001719D	36	28
0001726P	62	20
0001728Q	34	20
0001793Z	30	24
0001793Z	36	24
0001798P	66	6
0001799K	66	7
0001805G	18	16
0001805G	20	6
0001807Q	20	9
0001810T	20	15
0001811U	18	12
0001811U	20	4
0001823D	68	7
0001823D	68	26
0001823D	70	26
0001823D	74	26
0001824D	34	5
0001847G	36	17
0001858W	18	27
0001858W	20	26
0001858W	24	53
0001858W	30	39
0001858W	62	15
0001870Z	30	46
0001875T	62	16
0001875T	62	24
0001876F	10	16
0001876F	62	17
0001876F	80	44
0001884G	62	9

Codice	Pag.	Rif.
0001885C	62	8
0001942D	72	54
0001942D	76	54
0001942D	84	43
0001968Z	30	44
0001984A	20	28
0001985E	20	7
0001987N	20	5
0001988B	52	1
00021114E	62	4
0002115A	62	6
0002121A	34	17
0002138H	38	23
0002144H	20	25
0005135Z	68	4
0005135Z	68	23
0005316F	72	74
0005316F	76	58
0005317B	90	17
0005317B	92	17
0005324Y	90	8
0610000D	16	1
0610001E	16	3
0610002J	16	2
0610002J	17	86
0610002J	17	88
0610002J	17	93
0610002J	83	10
0610004B	16	5
0610004B	16	5
0610005F	16	6
0610005F	16	6
0610006K	16	7
0610006K	16	7
0610007P	16	8
0610008C	16	9
0610009G	16	10
0610010S	16	11
0610011T	16	12
0610012F	16	13
0610013B	16	14
0610014Y	16	15
0610015U	16	16
0610016G	16	17
0610017C	16	18
0610018Z	16	19
0610019V	16	20
0610020T	16	21

Codice	Pag.	Rif.
06100021U	16	22
06100022G	16	23
06100023C	16	24
06100025V	16	25
06100025V	83	18
06100025V	89	2
06100026H	16	26
06100026H	83	19
06100027D	16	27
06100027D	17	98
06100027D	83	3
06100028S	16	28
06100029W	16	29
06100029W	17	89
06100029W	17	94
06100029W	83	12
06100030U	16	30
06100030U	17	90
06100030U	17	95
06100030U	83	11
06100031V	16	31
06100031V	83	16
06100032H	16	32
06100033D	16	33
06100034S	16	38
06100035W	16	39
06100036A	16	40
06100036A	83	15
06100037E	16	41
06100037E	83	14
06100038T	16	42
06100039X	16	43
06100040V	16	44
06100041W	16	45
06100042A	16	46
06100043E	16	47
06100044T	16	48
06100045X	16	49
06100046B	16	50
06100047F	16	51
06100048U	16	53
06100049Y	16	54
06100050W	16	55
06100051X	16	52
06100051X	83	9
06100052B	16	56
06100053F	16	57
06100053F	83	17

Codice	Pag.	Rif.
06100054U	16	58
06100054U	83	6
06100055Y	17	80
06100057G	16	60
06100058V	17	61
06100059Z	17	62
06100059Z	83	7
06100060X	17	64
06100061Y	17	63
06100062C	17	65
06100063G	17	66
06100063G	83	13
06100064V	17	67
06100065Z	17	68
06100066D	17	69
06100067H	17	70
06100068W	17	71
06100069S	17	72
06100070Y	17	73
06100070Y	83	8
06100071Z	17	74
06100072D	17	76
06100073H	17	77
06100074W	17	78
06100075S	17	79
06100076E	17	81
06100077A	89	3
06100078X	89	1
06100081A	16	34
06100081A	83	5
06100082N	16	35
06100082N	83	1
06100083J	16	36
06100083J	83	4
06100084F	16	37
06100084F	83	2
06100207A	16	4
06100208X	83	21
06100210M	17	75
06100211N	83	22
06100212S	17	84
06100213W	17	82
06100213W	83	20
06100214K	17	83
06100215P	17	85
0611313Z	82	1
0611428S	82	8
0611429W	82	7

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0611510U	82	11
0611511V	82	10
0611520V	82	9
0612021H	82	6
0615211Q	82	2
0615217Z	82	3
0615233S	72	80
0616032P	72	78
0616033K	82	5
0618011S	82	4
0618012E	82	12
0618033C	72	79
0618034Z	17	87
0618034Z	17	91
0618034Z	17	96
0618034Z	17	99
0618035V	16	59
0618035V	17	92
0618035V	17	97
0618035V	17	100
0620127X	28	AG
0620143Y	26	61
0620148N	32	AG
0620227Z	8	AP
0620228N	8	AP
0620233Z	40	97
0620234N	48	18
0620236V	42	AG
0620238P	44	AG
0620239K	44	AG
0620241J	46	AG
0620242V	46	AG
0620243S	46	AG
0620247T	76	AG
0620262Y	22	AG
0620267Y	34	AG
0620284R	72	AG
0620285X	8	AP
0620286B	8	AP
0636069A	34	1
0637754S	8	32
0643044F	92	46
0643045B	92	46
0643394H	56	AG
0645810P	54	AG
0646523N	68	AG
0646527P	10	AG
0646530E	8	AG

Codice	Pag.	Rif.
0646567K	78	AG
0646702Y	84	AG
0646705M	66	AG
0646921X	68	AG
0646929Z	66	AG
0674124N	14	AG
0674125J	14	30
0674127S	14	32
0674128P	14	31
0674174K	14	2
0674175P	14	1
0674183F	14	43
0674268M	14	21
0674268M	60	16
0674313U	10	37
0674314R	10	38
0674317V	12	11
0674317Y	14	12
0674317V	60	4
0674335P	90	26
0674335P	92	26
0674345Q	90	20
0674345Q	92	20
0674383B	60	6
0674552G	14	3
0676322H	92	63
0676328T	92	64
0676329X	92	62
0676330V	92	61
0678337Y	72	57
0678338M	72	55
0678338M	76	55
0678339R	72	56
0678341Q	90	10
0678345R	90	9
0678370J	90	6
0678370J	92	6
0678371K	90	31
0678371K	92	31
0678413F	92	23
0678416C	90	13
0678416C	92	13
0678417G	90	14
0678417G	92	14
0678421Y	90	30
0678422C	90	29
0678422C	92	29
0678434W	90	15

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Codice	Pag.	Rif.
0678434W	92	15
0678436E	90	16
0678436E	92	16
0678450S	76	59
0678470U	76	73
0678471V	72	72
0678471V	76	72
0678508A	86	68
0678508A	90	11
0678508A	92	11
0678509E	90	36
0678509E	92	36
0678514W	90	28
0678549W	90	25
0678550U	90	22
0678551V	90	24
0678552H	90	21
0678553D	72	60
0678556A	72	71
0678556A	76	71
0678561W	92	30
0678563F	90	23
0678566B	90	18
0678567F	90	19
0678581G	92	28
0678586M	92	27
0678598F	92	37
0678599B	92	8
0679900Y	92	9
067990020	92	39
06799003H	92	40
06799006E	92	54
06799007A	92	47
06799008X	90	32
06799008X	92	32
0679910M	92	19
0679911N	92	18
0679922T	76	60
0679923X	76	57
0679924L	76	74
0679957T	92	57
0680116G	48	57
0680116G	50	26
0680205H	92	52
0680220V	80	12
0680311X	8	42
0680311X	36	41
0680331Z	32	77

Codice	Pag.	Rif.
0680341S	32	88
0680341S	36	35
0680451E	8	35
0680490Q	40	80
0680506T	8	45
0680506T	40	83
0680534D	56	11
0680550G	48	46
0680550X	50	28
0680551F	80	21
0680593T	32	81
0682081W	26	63
0682160C	80	29
0682260E	8	38
0682260E	48	45
0682260E	50	31
0682260E	56	13
0682260E	80	23
0682456X	8	36
0682456X	40	81
0682456X	48	47
0682456X	50	29
0682456X	80	24
0682481V	80	28
0682560L	8	43
0682560L	36	40
0682865D	10	8
0682868A	32	90
0682868A	36	37
0682871D	90	35
0682871D	92	35
0683040M	48	58
0683040M	50	27
0683060P	92	53
0683061Q	32	78
0683061Q	36	38
0683066W	80	30
0683081S	56	12
0683085T	32	89
0683085T	36	36
0683086F	8	37
0683086F	40	82
0683086F	48	44
0683086F	50	30
0683086F	80	22
0683092F	32	82
0683131E	8	44
0683131E	80	27

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Codice	Pag.	Rif.
0683505Y	32	79
0683542T	10	7
0683545Q	26	64
0689568H	84	21
0800796H	68	11
0800817U	68	30
0816165A	88	2
0817004A	92	55
0817007N	92	58
0817011S	92	56
0817036H	14	8
0817036H	60	1
0817043D	14	38
0817043D	60	8
0817045W	14	36
0817045W	60	12
0817073G	14	19
0817073G	60	13
0817075Z	60	7
0817081W	14	37
0817083R	14	22
0817083R	60	15
0817113T	14	17
0817490G	14	18
0817810R	92	59
0817811J	92	60
0817812W	92	22
0817813S	92	24
0817814P	92	21
0817815K	92	25
0819139G	14	4
0819140E	14	5
0819141K	14	6
0819142K	14	7
0819152L	56	1
0819158E	84	15
0830388L	18	32
0830388L	20	35
0830388L	24	51
0830388L	30	27
0830388L	38	32
0830388L	38	45
0830390N	18	36
0830390N	20	37
0830390N	30	30
0830391P	18	37
0830391P	20	38
0830391P	30	31

Codice	Pag.	Rif.
0830392T	18	38
0830392T	20	39
0830392T	30	32
0830393X	18	39
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0830395Q	18	41
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0830396U	30	36
0830397Y	18	43
0830397Y	30	37
0830398M	18	44
0830398M	30	38
0830399R	18	45
0830399R	30	39
0830400T	18	46
0830400T	30	40
0830401U	30	41
0830512X	38	49
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0830512X	50	13
0831073Z	10	17
0831074N	10	18
0831075J	10	19
0831095U	80	20
0831096G	80	25
0831766S	38	25
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0831792C	70	43
0831792C	74	43
0831815C	70	42
0831815C	74	42
0831823L	70	30
0831823L	74	30
0831825D	70	41
0831825D	74	41
0831836J	78	8
0831837N	78	9
0831845F	78	10
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0831847P	78	12

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0832950M	24	AP
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0833361M	32	93
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0834000S	18	26
0834000S	24	50
0834000S	84	59
0834000S	80	10
0834000S	6	25
0834007C	6	26
0834009V	6	24
0834189J	6	19
0834189J	80	31
0834229E	20	31
0834229E	80	7
0834397M	56	14
0834397M	78	33
0834416U	56	15
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0834614Q	90	1
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0834618R	90	3
0834618R	92	3
0834619M	90	4
0834619M	92	4
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08346610	78	5
0834662U	6	7
0834662U	8	52
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0834662U	30	20
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0834662U	36	40

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0834663Y	12	15
0834663Y	20	2
0834663Y	24	35
0834663Y	30	21
0834663Y	36	2
0834663Y	38	41
0834663Y	62	27
0834663Y	78	21
0834663Y	80	33
0834665R	14	24
0834665R	38	43
0834665R	58	17
0834665R	64	14
0835132C	6	8
0835132C	8	51
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0835132C	24	34
0835132C	30	22
0835132C	36	3
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0835286F	12	10
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0835484X	38	46
083548120	14	29
0835830D	58	2
0835835F	14	20
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0835835F	60	14
0835852L	12	13
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0835863R	12	16
0835863R	14	16
0835863R	58	18

Codice	Pag.	Rit.
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08358758	64	12
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0835882X	14	14
0835892Z	58	7
0835901R	58	4
0835901R	64	4
0835910D	12	4
0835910D	14	7
0835910D	60	5
0835914B	12	4
0835943R	14	4
0835943R	58	10
0835944E	64	9
0835944E	58	9
0835944E	64	9
0835949B	12	8
0835949B	58	1
0835949B	64	1
08359720	64	1
0835975B	58	3
0836220U	60	12
0836220U	64	10
08362264N	12	12
08362264M	14	10
08362264M	80	10
08362268N	12	9
08362268N	64	7
08362278P	64	3
08362280Z	12	6
08362284X	58	2
08362286F	64	11
08362286F	14	11
08362290S	60	3
08362291T	58	13
08362293B	12	7
08362293B	58	45
08362293B	80	48
08362405B	12	4
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08362405B	58	20
08362405B	14	42
08362407M	58	6
08362407M	14	54
08362408A	58	6
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Codice	Pag.	Rit.
0836855M	26	68
0836856Z	24	45
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0836858J	26	74
0836859N	24	31
0836860L	24	29
0836861M	24	27
0836862Z	24	21
0836863Y	24	19
0836865N	24	1
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0836867I	24	8
0836868O	53	15
0836869I	84	60
0837001U	24	20
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08370016	84	13
08370019	84	12
08370020	84	7
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08370028T	84	8
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08370032A	84	4
08370033E	84	5
08370036B	84	30
08370037F	84	31
08370038Y	84	6
08370046C	84	1
08370043Y	20	43
08371160R	26	62
08371171K	48	60
08371172X	84	9
08371173T	40	96
08371180T	40	95
08371180T	18	49
08371218S	32	86
08371221M	40	02
08372263S	26	69
08372263V	26	26

Codice	Pag.	Rit.
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0837278K	18	48
0837398X	76	56
0837409G	10	9
0837412F	88	65
0837413B	88	64
0837414Y	88	63
0837415U	88	62
0837416G	88	61
0837417C	88	60
0837418Z	88	59
0837419V	88	58
0837420U	88	57
0837421U	88	56
0837422G	88	55
0837423C	88	54
0837424Z	88	53
0837425V	88	52
0837426H	88	51
0837427D	88	50
0837428S	88	49
0837429M	88	48
0837430U	88	47
0837431V	88	46
0837432H	88	45
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0837434S	88	43
0837435M	88	42
0837436A	88	41
0837437E	88	40
0837438T	88	39
0837439X	88	38
0837440V	88	37
0837441W	88	36
0837442A	88	35
0837443E	88	34
0837444T	88	33
0837445X	88	32
0837446B	88	31
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0837449Y	88	28
0837450M	88	27
0837451X	88	26
0837452B	88	25
0837453F	88	24
0837454U	88	23

Codice	Pag.	Rit.
0837455Y	88	22
0837456C	88	21
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0837459Z	88	18
0837460X	88	17
0837461Y	88	16
0837462C	88	15
0837463D	88	14
0837464V	88	13
0837465Z	88	12
0837466D	88	11
0837467H	88	10
0837468M	88	9
0837469S	88	8
0837470Y	88	7
0837471Z	88	6
0837472D	88	5
0837473M	88	4
0837474W	88	3
0837476E	88	1
0837478X	88	55
0837479E	88	59
0837519X	50	40
0837534U	88	29
0837540X	88	44
0837541Y	88	44
0837544V	88	51
08375614U	66	66
08375615Y	66	66
08375616C	66	66
08375634W	26	70
08375635S	78	19
08375636E	78	18
08375636Z	78	17
08375635V	70	39
08375665V	74	39
08375670U	8	29
08375671V	8	40
08375673D	8	46
08375679K	38	35
08375679P	38	35
08375678T	38	28
08375678R	38	28
08375678A	10	32
08375678F	10	32
08375678B	8	32
08375678	8	32

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0839245C	74	35
0839246Q	70	37
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0839247L	70	31
0839247L	74	31
0839250B	70	38
0839250B	74	38
0839254H	70	32
0839254H	74	32
0839255D	70	36
0839255D	74	36
0839256R	68	8
0839256R	68	27
0839256R	70	33
0839256R	74	33
0839257M	70	34
0839257M	74	34
0839263M	38	33
0839265E	40	90
0839268B	18	33
0839268B	24	52
0839346J	52	14
0839352J	40	103
0839353N	40	104
0839355F	30	58
0839355F	66	24
0839356K	18	31
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0839356K	40	86
0839357P	20	17
0839357P	24	39
0839360E	10	28
0839360E	78	2
0839360E	80	4
0839366L	38	21
0839367Q	38	20
0839368D	30	26
0839368D	36	26
0839374D	36	30

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0839379A	36	19
0839382V	36	20
0839418J	26	73
0839418J	78	29
0839419N	24	48
0839420L	38	39
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0839473S	6	10
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0839474P	6	12
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0839609V	6	4
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0839609V	92	50
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0839610P	80	37
0839610P	92	48
0839611Q	6	3
0839611Q	80	40
0839611Q	92	51
0839612U	6	5
0839612U	78	25
0839612U	80	38
0839612U	92	49
0839652Y	36	29
0839653U	10	27
0839653U	18	30
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0839653U	24	38
0839653U	30	25
0839653U	36	25
0839653U	38	22
0839653U	52	13
0839653U	66	23
0839653U	78	3
0839653U	80	3
0839716X	80	6
0839772W	6	11
0839772W	80	43
0839831F	22	2
0839831F	28	5
0839831F	32	94
0839833P	22	3
0839833P	28	4
0839939B	80	8
0842137U	30	5
0842182C	54	5

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08422214Q	70	AG
08422214Q	74	AG
08422216Y	70	AG
08422216Y	74	AG
08422217U	70	AG
08422217U	74	AG
08422218R	70	AG
08422218R	74	AG
08422219M	70	AG
08422219M	74	AG
08422233V	30	15
08422251P	78	27
08422252T	78	24
08422253X	72	49
08422254L	30	2
08422261Q	70	AG
08422261Q	74	AG
08422262V	70	AG
08422262V	74	AG
08422264M	72	58
08422270Q	70	AG
08422270Q	74	AG
08422272V	68	10
08422272V	68	29
08422391V	68	AP
08422487P	68	AP
08422487P	70	AG
08422487P	74	AG
08422511Z	68	AP
08422512D	68	1
08422512D	68	21
08422514W	40	98
08422531T	8	AG
08422532F	48	AG
08422533B	48	AG
08422534Y	48	AG
08422535V	50	AG
08422585H	52	18
08422590G	8	39
08422598F	8	AG
08422602J	8	AP
08422603N	8	AP
08422604B	8	10
08422609G	10	AP
08422616G	38	34
08422622G	50	1
08422638T	10	3
08422647F	8	1

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08422673H	66	AP
08422682N	78	AP
08422706M	84	AP
08422713D	84	AP
08422740X	84	AP
08422755S	8	48
08422777C	84	AP
08422780B	38	6
08422781C	38	5
08422865N	24	49
08422893G	48	1
08422948W	24	AG
08422948K	24	AP
08422949P	24	AP
08422951N	24	AP
08422983H	24	AG
0877041T	86	72
1952106D	18	23
1952133X	18	8
1952184Z	18	9
3443104P	66	25
3543104P	24	40
3543104P	28	3
3543105K	36	33
3543106X	56	16
3543119H	36	32
3838762X	30	13
4915012W	8	19
4922050Z	46	30
4922450Y	46	45
4922530Y	52	4
4922770Y	46	25
4922930R	32	99
4922930R	46	38
4923050V	34	15
4923050V	46	20
4923370L	28	39
4923370L	42	16
4923370L	44	11
4923370L	44	23
4923450U	22	23
4923450U	46	19
4923610V	22	20
4923690C	22	19
4923770U	22	13
4923770U	46	23
4923770U	68	13
4923850M	28	41

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Codice	Pag.	Rif.
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4 9 2 4 1 3 0 H	5 2	5
4 9 2 4 2 1 0 H	2 2	1 7
4 9 2 4 2 1 0 H	4 6	2 2
4 9 2 4 2 9 0 R	4 6	3 2
4 9 2 4 3 7 0 H	2 2	2 1
4 9 2 4 3 7 0 H	2 8	3 8
4 9 2 4 3 7 0 H	6 8	1 2
4 9 2 4 4 5 0 R	4 6	3 6
4 9 2 4 5 3 2 W	2 2	2 2
4 9 2 4 5 3 2 W	4 6	2 6
4 9 2 4 6 1 0 R	2 2	1 6
4 9 2 4 6 1 0 R	3 2	1 0 2
4 9 2 4 7 7 0 R	2 8	3 7
4 9 2 4 7 7 0 R	4 6	2 4
4 9 2 4 9 3 0 A	4 6	3 1
4 9 2 5 0 5 0 N	2 8	3 6
4 9 2 5 1 3 0 D	2 8	3 1
4 9 2 5 6 1 0 M	2 8	3 2
4 9 2 5 7 7 0 M	2 8	3 5
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4 9 3 2 9 2 5 K	4 4	2 5
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4 9 3 3 1 2 7 W	4 2	1 0
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4 9 3 3 1 2 7 W	4 4	2 4
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4 9 3 3 2 0 2 D	2 2	1 5
4 9 3 3 2 4 5 J	4 6	4 5
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4 9 3 3 9 2 6 T	4 4	2 2
4 9 3 3 9 6 7 T	4 4	2 1
4 9 3 3 9 6 7 T	4 4	2 2
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4961791T	42	8
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49618400	34	27
4962074V	34	28
4962198V	46	18
4962430S	50	5
4962555Y	46	16
4962902B	46	17
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4963071U	34	29
4963071U	66	15
4963551T	52	20
4964071R	44	9
4964073Z	28	30
4964146R	34	26
4971086B	48	17
4971086B	50	6
4971871E	48	16
4972756H	24	8
4972904R	48	15
4973076A	20	21
4973345Q	34	18
4973460S	24	32
4973471U	20	24
4973660W	42	33
4973750X	24	30
4973845U	42	25
4973846X	34	16
4973860K	24	9
4975846X	42	26
4990060X	18	13
4991070W	48	4
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4991300Y	42	17
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4993314T	48	6
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4993540C	48	2

Codice	Pag.	Rif.
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5038235P	30	17
5038518J	32	97
5038680C	38	8
5041050Z	8	18
5041160K	34	34
5041160K	46	47

Codice	Pag.	Rif.
5041355Q	46	46
5041355Q	48	19
5041355Q	50	3
5041560T	42	6
5041560Q	44	5
5041560T	46	11
5042437L	24	16
5042437L	38	9
5091062A	36	13
5104032A	18	20
5104032A	24	11
5104040W	84	48
5111222L	76	82
5114404Y	72	48
5114404Y	76	48
5141133J	48	35
5141133N	50	19
5141200L	24	12
5141201M	24	13
5141201N	84	44
5141204J	18	21
5141205N	18	22
5141500S	68	36
5141504Y	70	1
5141504Y	74	1
5168110F	66	5
5241302V	30	6
5241302W	48	39
5241302W	50	22
5250102Z	66	21
5254900K	24	2
5268052Z	38	36
5268054J	38	37
5268060M	38	38
5300060W	84	2
5326226X	36	7
5326640T	38	16
5361011M	18	4
5361011M	24	4
5361011M	30	49
5361011M	38	11
5361011M	70	45
5361011M	74	45
5361011M	84	46
5361011M	84	52
5363150R	18	3
5363150R	24	3
5363150R	30	47

Codice	Pag.	Rif.
5363150R	38	12
5363150R	84	47
5363152W	18	5
5363152W	24	6
5363152W	30	48
5363152W	38	10
5363152W	84	45
5363153S	18	6
5363153S	24	7
5363153S	84	49
5363154P	18	7
5363154P	24	5
5373100Z	38	31
5373102D	38	30
5373104X	38	29
5421000E	48	27
5421000E	50	10
5421002J	48	26
5421004B	48	25
5421100W	30	1
5427060F	54	6
5427068F	56	7
5441340N	40	93
5445086J	24	37
5455200V	36	18
5455202H	30	57
5455222X	38	14
5455224Q	38	13
5455226Y	50	7
5541340N	10	39
5541340N	32	91
5541340N	36	31
5610021W	32	72
5610021W	48	10
5610024T	48	11
5610026B	28	6
5610028U	28	7
5610030W	28	8
5612404R	86	61
5612430A	72	51
5612430A	76	51
5612438H	72	52
5612438H	76	52
5612439C	52	12
5612455E	62	19
5612540D	18	29
5612540D	26	55
5612540D	40	88

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Codice	Pag.	Rif.
5612544Q	10	25
5612544D	78	1
5612544B	80	2
5612987L	72	53
5612987L	76	53
5612989D	10	23
5612989D	78	4
5612989R	80	1
5612991R	52	11
5612994H	72	50
5612994H	76	50
5613329W	10	26
5613329W	32	65
5613329W	52	17
5613333D	20	13
5613333D	40	85
5613333D	52	16
5613333D	72	65
5613333D	76	65
56133347E	34	7
5613350W	10	24
5613350W	18	47
5613350W	20	12
5613350W	40	91
5613350W	52	15
5613350W	72	64
5613350W	76	64
5613364V	28	14
5613520F	20	14
5613569E	26	75
5613569E	30	61
5613569E	50	4
5613569E	66	17
5616413J	48	34
5616413J	50	18
5616415B	38	52
5616418G	48	30
5616418G	50	14
5616450D	48	31
5616450D	50	15
5616452J	48	32
5616452J	50	16
5616454B	48	33
5616454B	50	17
5616455F	38	57
5616457P	38	56
5616459G	38	55
5617255X	8	17

Codice	Pag.	Rif.
5617260W	28	2
5618052C	10	15
5618054V	30	18
5618054V	72	63
5618054W	76	80
5618056D	6	2
5618056D	30	19
5618056D	80	36
5618320N	18	50
5618320N	40	94
5812010W	48	42
5812010W	50	41
5812012B	48	43
5812012B	50	25
5814010F	28	23
5814010F	28	23
5822468S	22	32
5822468S	34	31
5822725X	22	33
5822725X	28	21
5822725X	34	30
5822725X	42	2
5822725X	42	24
5822725X	44	13
5822725X	66	16
5822829K	34	32
5822840S	28	19
5822840J	32	96
5823605B	8	21
5824032X	22	29
5824038R	22	28
5824782H	18	24
5824782H	42	34
5824782H	44	14
5826022D	18	25
5826022B	42	11
5826022D	46	8
5826398U	28	20
5826398U	42	3
5826511S	20	30
5826513A	20	29
5826513A	24	22
5826600E	22	27
5826832X	22	30
5826842Y	28	22
5826842Y	42	12
5826845M	42	4
5826845M	44	18

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Codice	Pag.	Rif.
5829020N	8	20
5831018K	34	41
5831301M	22	37
5831671N	46	1
5831761N	22	36
5833400E	46	4
5833575V	34	40
5835527Z	22	38
5835750N	22	35
5835750N	46	5
5835860A	22	34
5836000C	28	17
5836000C	48	38
5836000C	50	21
5836002R	48	37
5839081W	46	2
5884011X	28	42
5884011X	42	22
5884011X	44	10
62211103H	86	73
6307430Q	72	73
6307430Q	80	11
6311230Q	8	22
6311230Q	24	28
6311230Q	32	85
6311230Q	40	74
6311230Q	48	52
6311230Q	68	14
6311230Q	84	54
6311231R	6	13
6311231R	10	14
6311231R	24	33
6311231R	40	76
6311231R	50	36
6311231R	66	18
6311231R	68	31
6311231R	72	75
6311231R	76	75
6311231R	78	31
6311231R	84	22
6311232V	6	18
6311232V	8	24
6311232V	24	23
6311232V	28	11
6311232V	38	63
6311232V	80	32
6311233Z	6	14
6311233Z	8	53

Codice	Pag.	Rif.
6311233Z	48	54
6311233Z	50	39
6311234N	8	23
6311234N	26	58
6311234N	40	77
6311234N	86	69
6311236W	10	10
6311236W	40	92
6311242W	24	43
6311242W	50	35
6311243S	10	35
6311243S	48	56
6311243S	54	9
6311243S	56	9
6311243S	66	20
6311243S	90	27
6311244P	38	62
6311244P	72	66
6311244P	76	66
6311245K	10	22
6311245K	16	59
6311245K	40	87
6311245K	54	12
6311245K	66	11
6311245K	78	14
6311247T	72	70
6311247T	76	70
6311247T	80	5
63112480	80	17
6311256Y	38	64
6312725F	10	5
6312732K	8	26
6312732K	48	53
6312733P	54	14
6312733P	56	8
6312735G	14	39
6312735G	60	9
6312736L	40	75
6312743Q	90	37
6313100F	84	35
6313104D	84	40
6313113D	24	41
6313114S	90	33
6313114S	92	33
6313115W	84	33
6313115W	92	38
6313132B	6	20
6313132B	40	78

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Codice	Pag.	Rif.
6313132B	80	13
6313210W	14	25
6313710G	84	37
6314145N	80	26
6316110Z	84	36
6321103H	6	16
6321103H	8	27
6321103H	10	13
6321103H	24	42
6321103H	28	12
6321103H	40	70
6321103H	48	49
6321103H	50	32
6321103H	70	44
6321103H	76	77
6321103H	78	30
6321103H	80	46
6321104W	14	41
6321104W	40	67
6321104W	54	13
6321104W	60	11
6321104W	72	69
6321104W	76	69
6321104W	78	15
6321104W	80	19
6321105S	6	23
6321105S	40	73
6321105S	80	16
6321109H	68	9
6321109H	68	28
6321110M	14	28
6322104A	86	71
6331103A	6	15
6331103A	8	25
6331103A	24	25
6331103A	10	11
6331103A	28	45
6331103A	40	68
6331103A	48	51
6331103A	50	37
6331103A	68	15
6331103A	68	32
6331103A	72	76
6331103A	76	76
6331103N	80	45
6331103N	86	70
6331104X	14	35
6331104X	14	40

Codice	Pag.	Rif.
6331104X	26	65
6331104X	40	65
6331104X	54	11
6331104X	58	21
6331104X	60	10
6331104X	66	9
6331104X	72	67
6331104X	76	67
6331104X	78	16
6331104X	80	47
6331104X	84	34
6331105T	6	21
6331105T	32	83
6331105T	40	71
6331105T	80	14
6331108Y	38	50
6331108Y	84	24
6331110N	14	26
6332103N	6	17
6332103N	8	28
6332103N	10	12
6332103N	24	24
6332103N	40	69
6332103N	48	50
6332103N	50	33
6332103A	66	19
6332103N	68	16
6332103N	68	33
6332103N	76	81
6332103N	78	28
6332103M	84	53
6332104B	10	36
6332104B	24	44
6332104B	40	66
6332104B	48	55
6332104B	50	34
6332104B	56	10
6332104B	66	10
6332104D	72	68
6332104B	76	68
6332104X	80	18
6332104B	84	38
6332105F	6	22
6332105F	40	72
6332105F	80	15
6332110S	14	27
6332303J	28	13
6332304F	54	10

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Codice	Pag.	Rif.
6337106Q	26	71
6337106Q	38	46
6337106Q	78	23
6337107L	92	10
6337109D	84	23
6337111X	84	32
6337114V	84	25
6337116D	90	5
6337116D	92	5
6343080G	38	54
63800002Z	24	47
63800003V	24	46
6478500M	90	7
6478500M	92	7
7454744G	76	78
7454746Q	76	79
7454756R	84	39
7465700P	10	6
7465702U	26	56
7465706V	90	34
7465706V	92	34
9401020E	12	17
9401020E	14	15
9401020E	58	19
9401020E	64	16
9431035Y	90	12
9431035Y	92	12

[illegible]